DOCTORAL DISSERTATION

STUDY ON
ADVANCED LITHOGRAPHY TECHNIQUES USING SCANNING PROBE MICROSCOPY FOR FABRICATION OF NANOSCALE Si DEVICES

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Preface

Silicon-based microelectronic devices such as metal oxide semiconductor field-effect transistors (MOSFETs) play an important role for switching devices over the past decades. Recently, the observation of quantum point contact (QPC) and the discoveries of large magnetoresistance (MR) effects in nonmagnetic materials have much attention as novel functional devices. The observation of these effects in semiconductor is an important milestone towards new applications. Therefore, for the future, it is required that the electrical properties of the devices are easily controlled at nano- and micro-scales. Furthermore, the miniaturization of the devices found in integrated circuits is predicted by the semiconductor industry roadmap to atomic dimensions in the future. To overcome these problems, many experiments have previously been reported on nanofabrication, which involves scanning probe microscope (SPM) local oxidation, SPM scratch nanolithography, shadow evaporation, and electromigration. Especially, SPM local oxidation and scratch techniques can achieve atomic resolution on semiconductor and metallic surfaces. We investigate the improvement of SPM lithograohy at nano- and micro-scales, and control of the electrical properties of planar-type devices by using the SPM lithography.

The reaction mechanism of the SPM local oxidation is considered to be the anodic oxidation. Since the local oxidation using SPM requires the field-induced formation of water meniscus between a conductive SPM tip and material surface, a negative bias voltage is applied to the SPM tip. Consequently, the water meniscus connects the SPM tip and the material surface and creates oxyanions (OH^-, O^-) from water molecules. These oxyanions act as reaction species in order to form the oxide at nano- and micro- scales. On the other hand, by using the SPM tip with a sufficient force, materials can be removed from the surface of the sample and then grooves can be produced. SPM scratching is regarded as a direct patterning

and resistless lithography, where a tip is used to provide local friction on the sample to modify the surfaces.

In this dissertation, in order to clear the mechanism of SPM local oxidation, we have a comparative study of contact and tapping mode SPM local oxidation experiments with the same SPM tip. The feature size of Si oxide wires was well controlled by varying the oscillation amplitude and Q-factor of the cantilever in tapping mode operation. Additionally, we estimate the oxidation ratio and rate constant for the fabrication of Si oxide wires with 10 nm resolution. Under the same oxidation conditions with the same SPM tip, the average full width at half maximum (FWHM) and the standard deviations (STDs) of the Si oxide wire fabricated by tapping mode oxidation are 11.0 nm and 2.1 nm, respectively, which are smaller than those of contact mode oxidation. Moreover, minimum FWHM is estimated to be 8.5 nm. Then, we exhibited the model of tapping mode SPM local oxidation based on the oxidation ratio and the rate constant. From the model, the oxidation ratio is estimated to be 10-16 % in tapping mode oxidation with 10 nm resolution. The rate constants of tapping mode oxidation are larger than those of contact mode oxidation, which suggests the formation of small and uniform oxide in tapping mode operation.

Micrometer-scale SPM local oxidation lithography was also performed on Si. In order to realize large-scale oxidation, an SPM tip with a contact length of 15 μm was prepared by focused-ion-beam (FIB) etching. Then, the Si oxide in the width of over 10 μm is easily fabricated by SPM local oxidation. Furthermore, the throughput of large-scale oxidation reached about 10^3 $\mu m^2/s$ by controlling the scanning speed and contact force of the SPM tip. It is suggested that SPM local oxidation can be upscaled by using a SPM tip with large contact length.

In the SPM scratching of a Si surface using a diamond-coated tip, groove size is well controlled by the applied force. A minimum width of 11 nm was successfully achieved. The

STD varied between 1.09 and 2.0 nm in width and between 0.04 and 0.3 nm in depth. Furthermore, size fluctuation of the grooves, determined in terms of relative STDs (RSDs) is approximately 10 % without depending on the applied normal force and can be suppressed considerably. Furthermore, the conductance of the Si channel is easily controlled by the SPM scratching.

On the other hand, we also propose that the electrical properties of planar-type devices are easily controlled by using SPM lithography at nano- and micro-scales. To investigate the control of the conductance between source and drain of the planar-type devices, SPM scratch nanolithography were performed for the fabrication of Au and Si channel. Furthermore, MR effects of Si planar-type devices were studied. In Au channel, conductance plateau below 12 G_0 ($G_0 = 2e^2/h$) is clearly observed. Moreover, the drain current of Si planar-type devices is easily controlled by SPM scratch nanolithography. It is concluded that the scratch nanolithography using SPM is useful for the control of planar-type Si devices.

We also investigate the MR effect of silicon-on-insulator (SOI) substrates with the aim towards its application to electronic devices. At room temperature, SOI substrate show positive MR of 15 %. Furthermore, we fabricate the planar-type Si devices with SOI substrates. These devices show MR of 1.1 % at room temperature. Here, it is considered that MR of Si devices strongly depend on the carrier concentration, carrier mobility, and channel geometries (gate width and length). SPM local oxidation and scratching techniques are useful for fabricating the constriction of the channel at nano- and micro-scales. Therefore, SPM lithography techniques and MR effect in Si devices can be utilized to develop advanced silicon based electronics technologies.

Table of Contents

Chapter 1

Overview and Objective of This Research

Scanning probe microscopy (SPM) systems, such as atomic force microscopy (AFM) and scanning tunneling microscopy (STM), are not only useful for the evaluation of surfaces, but are also promising candidates for nanolithographic tools because of their operational versatility and simplicity. Local oxidation nanolithography using SPM has enabled us to fabricate nanometer-scale oxide wires on material surfaces [1]. It is well known that an external voltage applied between SPM tip and sample locally induces the anodic oxidation on the surface. Silicon [2], titanium [3] and niobium [4] surfaces have been locally oxidized by the SPMs such as STM and AFM. It is considered that SPM local oxidation is a novel nanolithography technique for fabricating single-electron transistors (SETs) [5], metal-insulator-metal (MIM) diodes [6] and planar-type ferromagnetic tunnel junctions [7]. Several SPM modes, such as contact, noncontact and tapping, have been used to perform local oxidation nanolithography. Local oxidation using contact mode is the most extended method for SPM nanolithography techniques. It has been reported that the use of tapping mode SPMs to locally oxidize the surfaces is also available as a nanolithography tool in order to obtain a precise control of the oxidation on the nanometer scale and to improve the reproducibility of the oxidation process [8-10]. However, in view of device applications, it is considered that conventional SPM-based nanolithography is not suitable in terms of the fabrication throughput because nanometer-scale devices such as SETs are composed of submicrometer-scale current confinement structures and micrometer-scale device separation/isolation regions. Thus, both nanometer-scale and micrometer-scale SPM local oxidations are required. However, the sub 10-nm nanolithography and micrometer-scale SPM

local oxidation have not yet been reported. Furthermore, it has not also been described that the analytical model of SPM local oxidation for fabricating the nanometer-scale oxidation.

On the other hand, one interesting and promising method using SPM-based nanolithography techniques is the mechanical scratching of surfaces with a SPM tip [11,12]. This technique has been used on various specimens [13-17]. It is possible to carry out the nanometer scratching of soft materials such as poly-(methyl methacrylate) (PMMA) [13], polycarbonate [14], GaSb [15], and GaAs [16] using a Si or Si3N4 tip, which typically has a radius of approximately 20 nm. In contrast, on a hard material such a Si, we usually use a diamond tip with extremely high wear resistance [18-21]. A groove with a 35 nm width has been fabricated on Si surfaces using a diamond tip [21]. However, the sub-20 nm nanolithography of Si using SPM scratching has not yet been reported.

Although SETs are promising candidate for new nano-scale devices due to the good scalability as well as the low power property, magnetoresistance (MR) effects in ferromagnetic tunnel junctions have generated considerable interest due to their application in magnetic data storage / memory devices [22, 23]. Furthermore, in recent years, spin-transistors with semiconductor and ferromagnetic materials [24-29] have received considerable attention as a highly-functional building block of future integrated circuits [28-30]. In order to realize spin-transistors, it is essential that efficient spin injection/detection for their semiconductor channel is established [31-35]. Moreover, spin-transistors using an ordinary metal-oxide-semiconductor field-effect-transistor (MOSFET) and magnetic tunnel junctions are proposed [36]. However, this is not so easy in practice owing to several problems related to the ferromagnetic/semiconductor interfaces, such as interfacial layer formation, Fermi level pinning, and conductivity mismatch problems [31, 35, 37]. Although feasible technologies for these interface problems have been explored so far, definitive solutions for them are still at the stage of searching.

In contrast, research on magnetotransport of semiconductors without using magnetic materials is a field of increasing interest. The summary of MR effects without magnetic materials. The MnSb granular films of magnetic semiconductors are well kwon for the observation of MR effects, and 1,000 % MR is measured at 0.5 T [38]. Recently, nonmagnetic materials such as InSb exhibit geometric MR, which is an order of magnitude larger than the physical MR of other materials [39]. Furthermore, large positive MR effects were also reported in several nonmagnetic semiconductors such as Au/semi-insulating GaAs Schottky diode [40], B-doped Si [41]. These behaviors are caused by a magnetic-field-controlled impact ionization of carriers. In 2009, it has been found that P-doped Si shows a large positive MR between 0 and 3 T of more than 1,000 % at 300 K and 10,000 % at 25 K [42]. This phenomenon can be explained by the quasi-neutrality breaking of the space-charge effect, where insufficient charge is present to compensate the electrons injected into the device [43, 44].

The observation of a large MR in Si based on this phenomenon is an important milestone towards new spintronics applications. Actually, for sensing application, there is a Corbino disk which consists of InSb with high electron mobility of 78000 $cm^2/V \cdot s$ [45]. With the aim towards its application to electronic devices, the MR of a two-dimensional electron gas in a disordered Si (metal-oxide-semiconductor field-effect-transistor (Si-MOSFET)) is measured at a magnetic field of 40 T [46]. In this device, the MR of 100 % was obtained since the MR was considered as a result of modified scattering due to screening and density of states modifications caused by the spin polarization of the two-dimensional electron gas [47]. Furthermore, the Si-MOSFET structure exhibits a positive MR of about 18 % at room temperature with a magnetic field of 9 T, due to the presence of high-mobility electrons in the Si inversion layer [48]. These reports imply that new functional Si devices with MR effects are candidate for next-generation devices.

In this dissertation, simple and easy nanolithography techniques for fabrication of nanometer-scale devices using SPM lithography are investigated, and advanced Si devices with MR effects are studied. There are seven chapters through this dissertation, and overview of this dissertation is shown in Fig. 1.1. Following this chapter, theoretical prospect of MR effects in nonmagnetic materials are described in Chapter 2. In this chapter, the principle of MR effects with nonmagnetic materials and MOSFET are mentioned. Furthermore, transverse MR effect in Si substrate and the MR induced by a geometrical effect is also described.

Chapter 3 shows SPM local oxidation lithography at micro- and nano-scale. In this chapter, we investigate the size dependence of the wires on the dynamic properties (oscillation amplitude, Q-factor) of the cantilever used in tapping-mode SPM local oxidation nanolithography. Furthermore, we also have a comparative study between tapping and contact mode SPM local oxidation nanolithography using the same SPM tip. In addition, we quantitatively explained the size of the oxide controlled with tapping mode local oxidation nanolithography using a model based on the oxidation ratio and the rate constant of the oxidation reaction. These results imply that tapping mode SPM local oxidation is a suitable technique for the fabrication of nanometer-scale Si oxide wires with higher controllability and better size uniformity. On the other hand, micrometer-scale scanning probe microscopy (SPM) local oxidation lithography was performed on Si. It is suggested that SPM local oxidation can be upscaled by using a SPM tip with large contact length.

Chapter 4 describes SPM scratching performed at low force regime below 9 μN with a diamond coated tip on Si surface. The groove patterns with controlled width and depth could be achieved by adjusting the applied force, scan direction and the number of scan cycles. Furthermore, the wear coefficient of Si (100) was calculated using Archard's wear law. These results suggest that the SPM scratching could be a key technique for the fabrication of nanoscale devices with 10 nm dimensions.

In Chapter 5, SPM scratch nanolithography is used for the control of the conductance of planar Si devices. The results show that the conductance of the Si channel is easily controlled by the SPM scratching. Furthermore, SPM scratching nanolithography was applied to Au nanochannels for control of device properties of planar-type devices with in-situ measurement. The conductance plateau was clearly observed below 12 G_0. These results suggested that the electrical properties of planar-type devices are easily controlled by SPM scratch nanolithography techniques. MR effects in planar-type Si devices are also described in Chapter 5. The devise was patterned on silicon-on-insulator (SOI) substrate by electron beam lithography and wet etching process. MR of SOI substrate is investigated at 300 K, and then, the MR of planar-type Si devices is measured. Furthermore, SPM nanoscratching lithography is utilized to investigate the MR effects in planar-type Si devices at 300 K.

Lastly, concluding remarks of this study are summarized in Chapter 6.

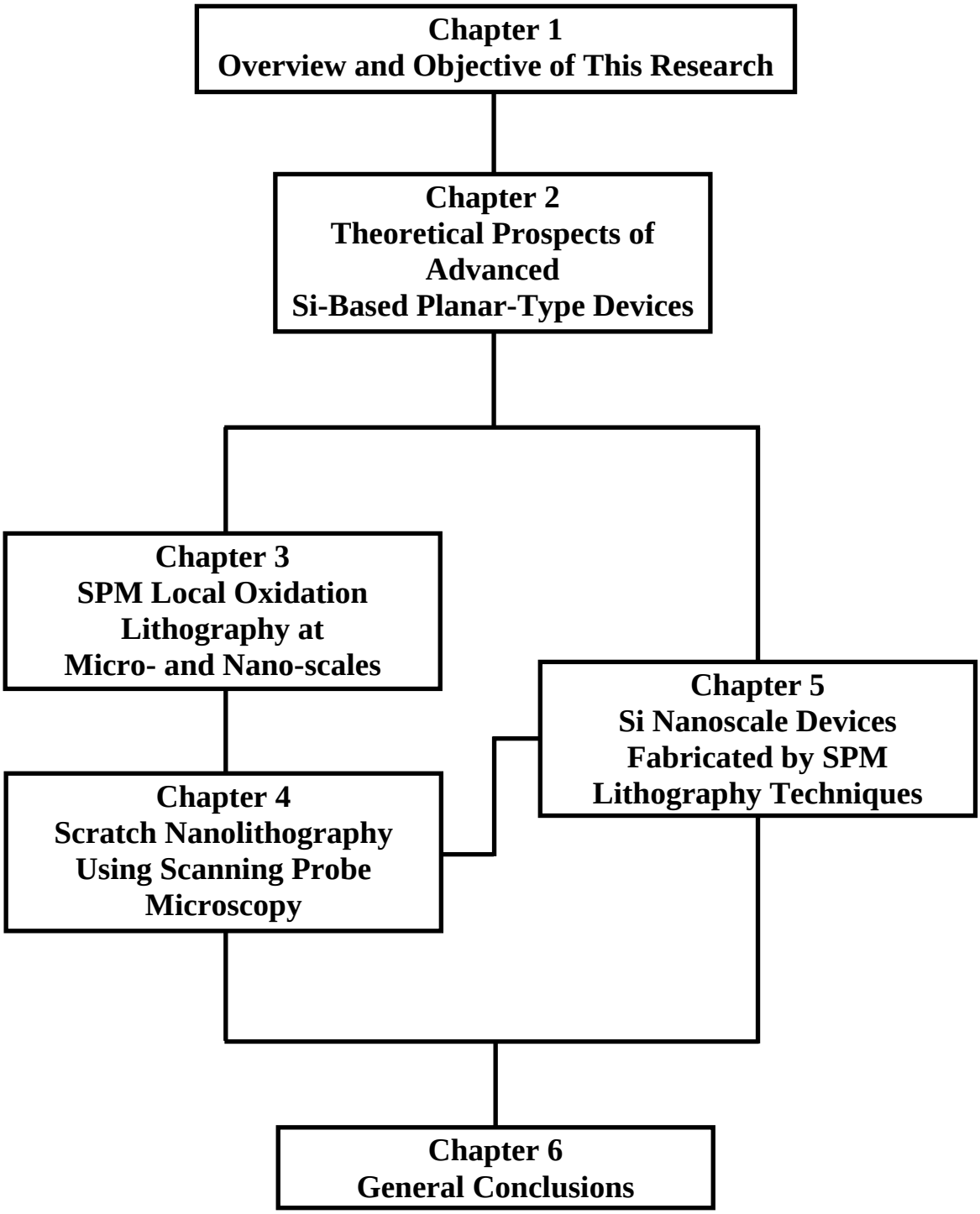


Fig. 1.1. Overview of this research.

Chapter 2

Theoretical Prospects of Advanced Si-Based Planar-Type Devices

2.1 Introduction

The patterning of semiconductor surfaces is a key technology for the development of micro- and nano-scale electronic devices. Further shrinkage of the devices requires the development of new lithographic techniques. Various possibilities are performed such as techniques based on electron beam [1], ion-beam [2-4] and scanning probe lithographies [5-7]. These various approaches can be used either to sensitize a resist layer or to directly pattern the surface in the nanometer range. Several resistless techniques have the drawback of being sequential but have the advantage to bypass all the spin coating, development and removing steps but they are still in the exploratory stage.

Since scanning probe microscopes possess potentially the highest lateral resolution, their use for high resolution patterning has been widely investigated, see Ref. [5-12]. Dagata et al. first with Scanning Tunnel Microscopy (STM) [13], then Snow and Campbell with a conductive Atomic Force Microscopy (AFM) [14] have described a direct oxide writing process using local depassivation of H-terminated Si in moist air by applying an anodic voltage between the SPM tip and the substrate. High lateral resolution structures and devices can be built using these approaches not only on Si but also on other semiconductors such as GaAs and InAs [15] or metals such as Cr, and Al [16-17].

AFM micro- and nano-machining of surface is also possible by direct matter removing by indentation or scratching process [18] or by tip induced selective dissolution [19]. Due to its efficient cost performance capability, SPM lithography plays an important role in the fabrication of electrical devices. Therefore, the combination of the various electrical

properties with SPM-based surface modifications is candidate for semiconductor nano-structuring process.

In this dissertation, we performed the control of electrical properties such as the quantum state and magnetoresistance (MR) effects in semiconductor by using SPM lithography. In this captor, introduction of SPM lithography and the MR effects in nonmagnetic material such as silicon and other semiconductor was described.

2.2 Planar-Type Devises Fabricated by SPM Lithography

Recently, there are several lithography techniques using scanning probe microscopy (SPM). In this chapter, SPM local oxidation lithography and SPM scratching nanolithography techniques were described as shown in Fig. 2.1. Local oxidation nanolithography using SPM has been widely used to produce nanometer-scale structures on the substrate surface [20]. This technique is recognized as possible nanofabrication tools for nanoelectronic applications such as single-electron transistors [21, 22] and planar-type ferromagnetic tunnel junctions [23, 24]. In general, the feature size of the oxide is strongly affected by the size of the water meniscus [25], relative humidity [26], applied bias voltage [27], scanning speed of the SPM cantilever [27], and operation mode [28]. It is also known that the voltage modulation in contact mode SPM local oxidation overcomes the self-limiting property of the oxidation by eliminating the buildup of space charges within the oxide during growth [29]. In this dissertation, we proposed the SPM local oxidation with active control of cantilever dynamics such as amplitude modulation and quality factor of cantilever for producing higher controllability and uniformity on the nanometer-scale fabrication of Si oxide wires. Furthermore, micrometer-scale lithography is performed in this study by using the "micrometer tip" which has a robust blunt tip.

On the other hand, the mechanical scratching using SPM is a powerful tool for the modification of surfaces on the nanometer scale [30, 31]. By rising contact force between the tip and sample, hole or groove structures can be directly patterned on the sample. Since no further processing like resist development or etching is required, direct patterning using SPM scratching attracts a good deal of interest. A variety of structures, including holes, grooves and square areas, was generated on various specimens [32-34]. Recently, a minimum groove width of 7 nm has been mechanically patterned on GaAs surface using a typical Si_3N_4 tip [35]. In the case of soft materials, since the hardness of these materials is much less than Si or

Si_3N_4, the nanometer scratching can be easily achieved using a Si or Si_3N_4 tip with a typical radius of less than 20 nm. The resolution in SPM-based nanolithography is essentially limited by the tip radius. In case of a hard material such a Si, a diamond tip with extremely high wear resistance should be used [36-39]. The radius of the diamond tip generally becomes larger because of the polycrystalline diamond coating on the tip side of the Si cantilever. Therefore, it is probably difficult to obtain nanoscale patterns on Si using SPM scratching. In the study, a commercial diamond tip was used, without further sharpening of the tip. Thus, not only tip radius but also applied force is important for the determination of the resolution of SPM scratching. In this dissertation, we systematically analyzed how scan parameters such as applied force, scan direction, scan speed and the number of scan cycles affect the width and depth of the fabricated grooves. Using this technique, more complex nanostructures such as line and space patterns and quantum dot arrays were demonstrated on Si surfaces.

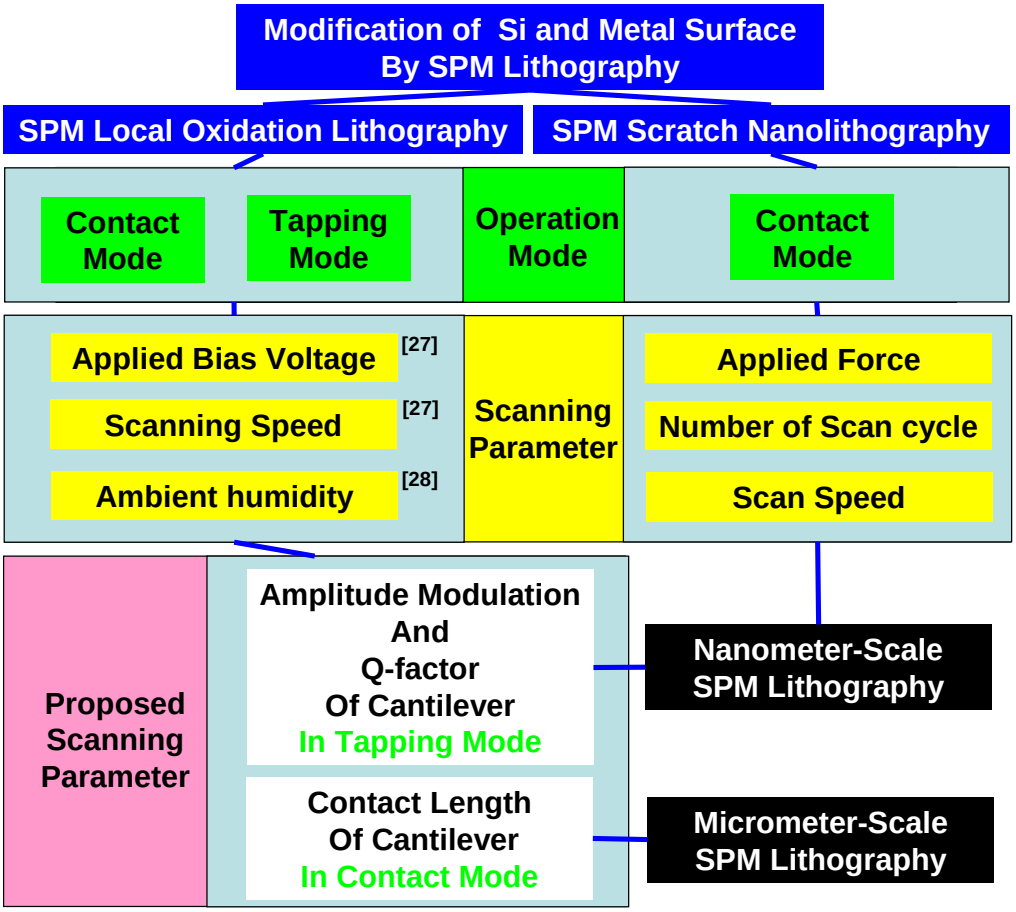


Fig. 2.1. SPM local oxidation lithography and SPM scratching nanolithography of SPM Lithography techniques.

SPM lithography techniques have been utilized for fabrication of the devices. For example, it has been demonstrated that the use of AFM anodic oxidation of Al films guided by in- situ electrical measurements for the fabrication of atomic-sized metallic point contacts as shown in Fig. 2.2(a) [40]. Figure 2.2(b) exhibits that the one-dimensional character of the electronic transport is evidenced by the discrete steps in conductance as the point contact is formed. At present, the relatively long time for the system to reach equilibrium inhibits fabrication of point contacts with reproducible conductance. This method could be used for fabricating nanometer-scale quantum effect devices.

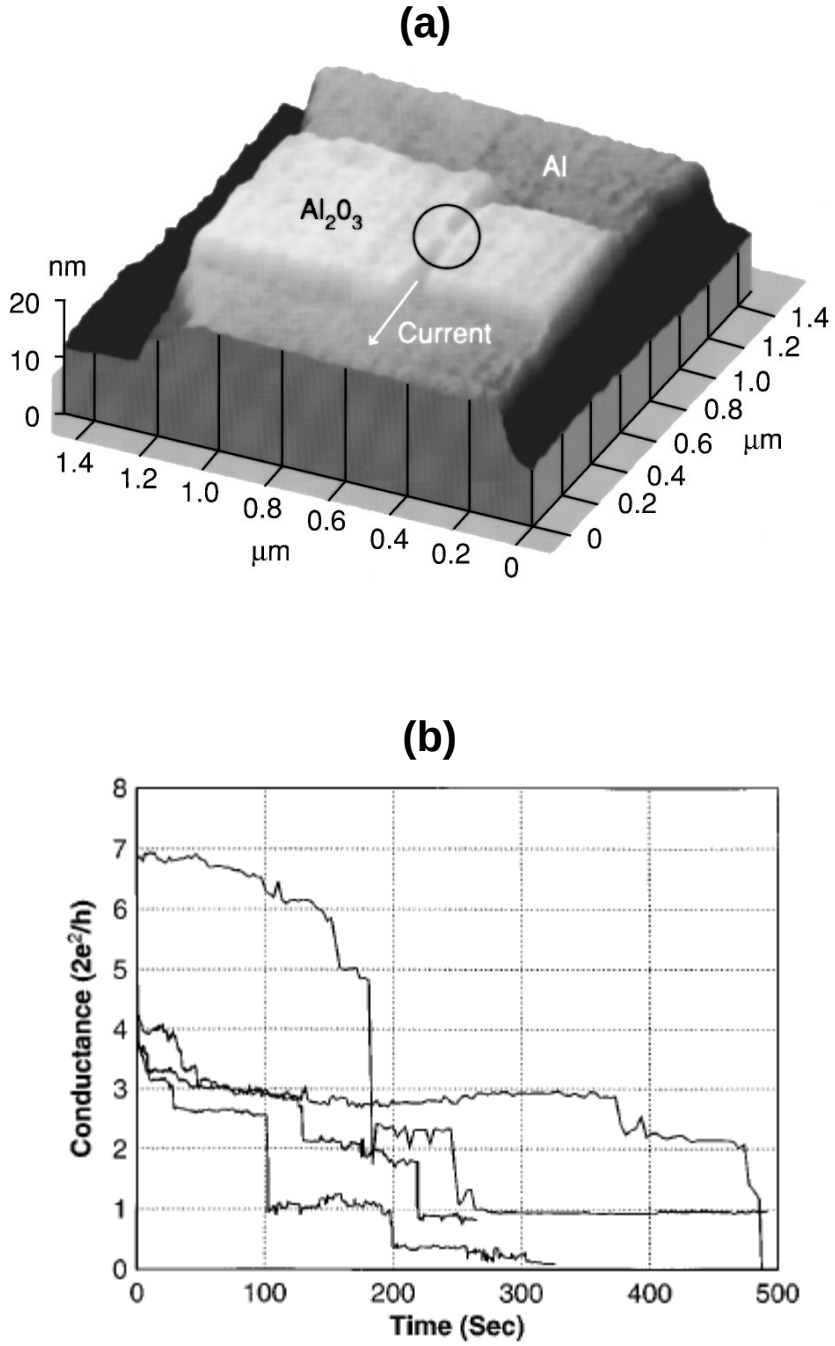


Fig. 2.2. (a) AFM image of a point contact device. (b) Records of the conductance recorded a function of time for four devices immediately after the tip voltage is set to zero [40].

2.3 Spin Transport in Silicon

The spin lifetime and diffusion length of electrons are transport parameters that define the scale of coherence in spintronics devices and circuits. As these parameters are many orders of magnitude larger in semiconductors than in metals [41, 42], semiconductors could be the most suitable for spintronics. So far, spin transport has only been measured in direct-bandgap semiconductors [43-49] or in combination with magnetic semiconductors, excluding a wide range of non-magnetic semiconductors with indirect bandgaps. Most notable in this group is silicon, Si, which (in addition to its market entrenchment in electronics) has long been predicted a superior semiconductor for spintronics with enhanced lifetime and transport length due to low spin–orbit scattering and lattice inversion symmetry [50-52]. Despite this promise, a demonstration of coherent spin transport in Si has remained elusive, because most experiments focused on magnetoresistive devices; these methods fail because of a fundamental impedance mismatch between ferromagnetic metal and semiconductor [53], and measurements are obscured by other magnetoelectronic effects [54].

Here, Appelbaum et. al demonstrate conduction-band spin transport across 10 *m*m undoped Si in a device that operates by spin-dependent ballistic hot-electron filtering through ferromagnetic thin films for both spin injection and spin detection [55]. As it is not based on magnetoresistance, the hot-electron spin injection and spin detection avoids impedance mismatch issues and prevents interference from parasitic effects. The clean collector current shows independent magnetic and electrical control of spin precession, and thus confirms spin coherent drift in the conduction band of silicon.

Figure 2.3(a) illustrates the operating principle and schematic band diagram of the device. Spin injection and detection is based on the attenuation of minority-spin hot electrons in ferromagnetic thin films, as in spin-valve transistors [56, 57]. In the device, the spin-valve transistors used for injection and detection each only have a single ferromagnetic base layer,

and we define these as ‘hot-electron spin transistors’. In step 1, a solid-state tunnel junction injects unpolarized hot electrons from the Al emitter into the ferromagnetic $Co_{84}Fe_{16}$ base, forming emitter current Ie. Spin-dependent hotelectron scattering attenuates minority spin electrons (step 2), so that the electrons transported over the Schottky barrier and into the undoped single-crystal float-zone (FZ)-Si conduction band (forming injected current Ic_1, the ‘first collector current’) are polarized, with their spin parallel to the magnetization of the $Co_{84}Fe_{16}$ (step 3) [58]. After vertical transport through the 10-mm-thick undoped Si (step 4), the spin polarization of the conduction-band electrons is detected by a second hot-electron spin transistor. The $Ni_{80}Fe_{20}$ base again uses ballistic hot-electron spin filtering, so the ‘second collector current’ (Ic_2, step 5) formed from ballistic transport through the $Ni_{80}Fe_{20}$ and into the n-Si substrate conduction band is dependent on the relative magnetizations of both ferromagnetic layers. When they are parallel, Ic_2 is higher than when they are antiparallel, but only if electron spinpolarization is maintained through the undoped Si layer. Therefore, this device is the electron analogue of the photon polarizationanalyser experiment in optics. There are various intrinsic device aspects that allow a clean spin transport signal in Ic_2, and that make it immune to fringe fieldinduced magnetoresistance and Hall effects.

In Fig. 2.3(b), in-plane magnetic hysteresis data of Ic_2 at Ve = -1.8 V and 85 K are shown. Measurements begin with fully saturated and aligned magnetizations by ramping to our magnetic field maximum. When the magnetic field is swept through zero and changes sign, first the $Ni_{80}Fe_{20}$ switches to align with the field and the magnetizations are antiparallel, resulting in a reduction in Ic_2 of approximately 2 %.

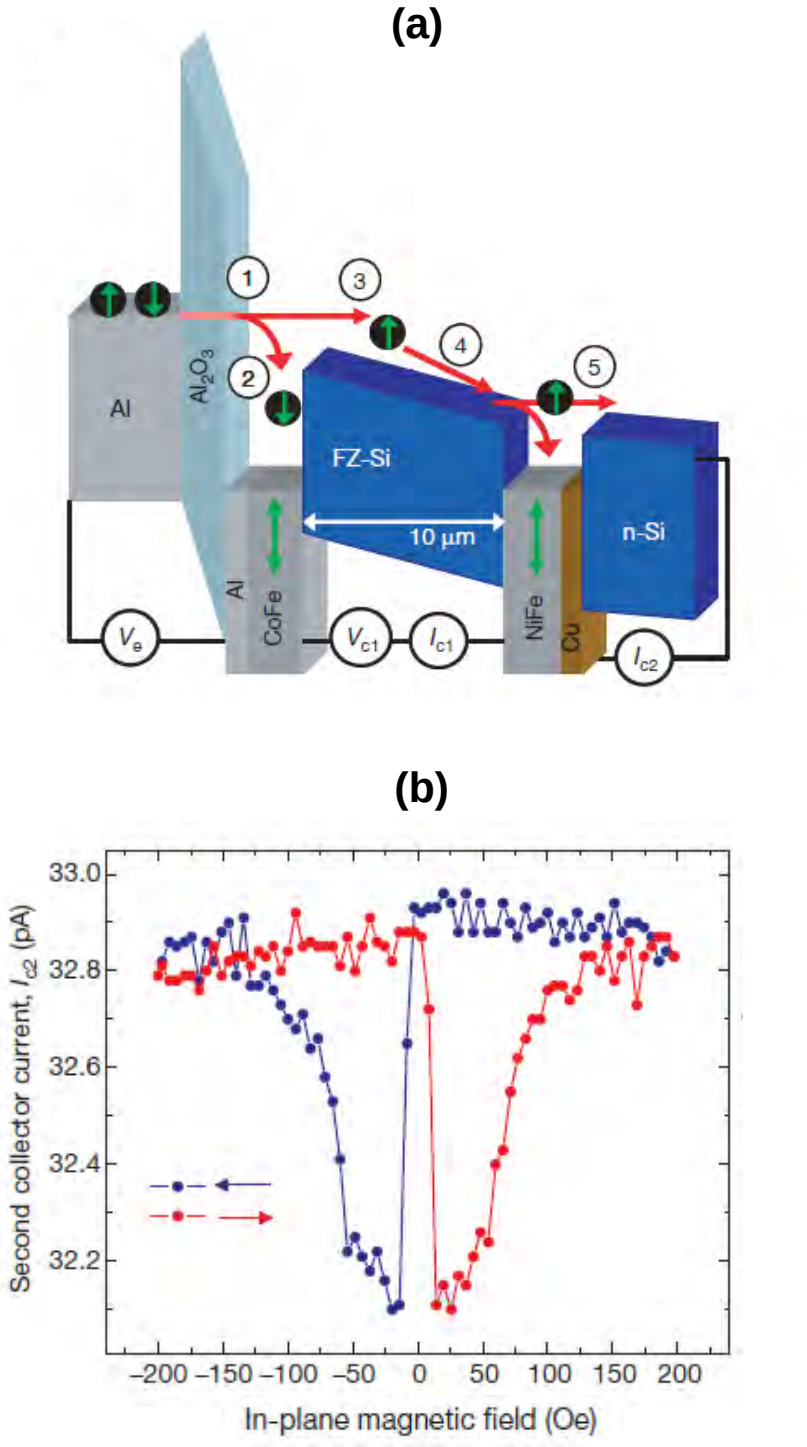


Fig. 2.3. (a) Illustration of the Si spin transport device. (b) In-plane magnetic field dependence at 85K [55].

Spin transistors, which utilize two ferromagnetic layers as a spin injector and a spin analyzer, possess unique output characteristics that are controlled by the relative magnetization configuration of the ferromagnets as well as the bias conditions [59]. Also, the magnetization in spin transistors can be used as nonvolatile binary data. Owing to these useful features, spin transistors are potentially applicable to integrated circuits for ultrahigh-density nonvolatile memory whose memory cell is made of a single spin transistor and for nonvolatile reconfigurable logic based on functional spin transistor gates. In order to realize such spintronic integrated circuits with high performance, the following requirements must be satisfied for spin transistors: (i) large magnetocurrent ratio for nonvolatile memory and logic functions, (ii) high transconductance for high speed operation, (iii) high amplification capability voltage, current and/or power gains to restore propagating signals between transistors, (iv) small power-delay product and small off-current for low power dissipation, and (v) simple device structure for high degree of integration and high process yield. Although various spin transistors have been proposed so far [59, 60] none of them can satisfy all of these requirements. Especially, the high transconductance and amplification capability cannot be realized simultaneously with the large magnetocurrent ratio. Sugahara et. al. propose and theoretically analyze a metal–oxide–semiconductor FET MOSFET type of spin transistor, hereafter referred to as a spin MOSFET, consisting of a MOS structure and half-metallic-ferromagnet (HMF) contacts for the source and drain. The proposed spin MOSFET can simultaneously satisfy all the above-described requirements [61].

As shown in Fig. 2.4(a) and (b), when the magnetization configuration of the HMF source and drain is parallel (antiparallel), highly spin-polarized carriers injected from the HMF source to the channel are transported into (blocked by) the HMF drain, resulting in the magnetization-configuration-dependent output characteristics. Here, the magnetocurrent ratio of the spin MOSFET is defined by $(I_D^P - I_D^{AP})/I_D^{AP}$. The symbols of I_D^P and I_D^{AP} show the

current in parallel and antiparallel magnetization, respectively. Two-dimensional numerical analysis indicates that the spin MOSFET exhibits high (low) current drive capability in the parallel (antiparallel) magnetization, and that extremely large magnetocurrent ratios can be obtained as shown in Fig. 2.4(c). From the figure, magnetocurrent ratio more than 1000 % can be obtained for source-drain voltage (V_{DS}) less than 1.0 V at the gate voltage (V_{GS}) of 1.5 V. These results show the spin MOSFET satisfies other important requirements for spintronic integrated circuits and useful for the spin transistors.

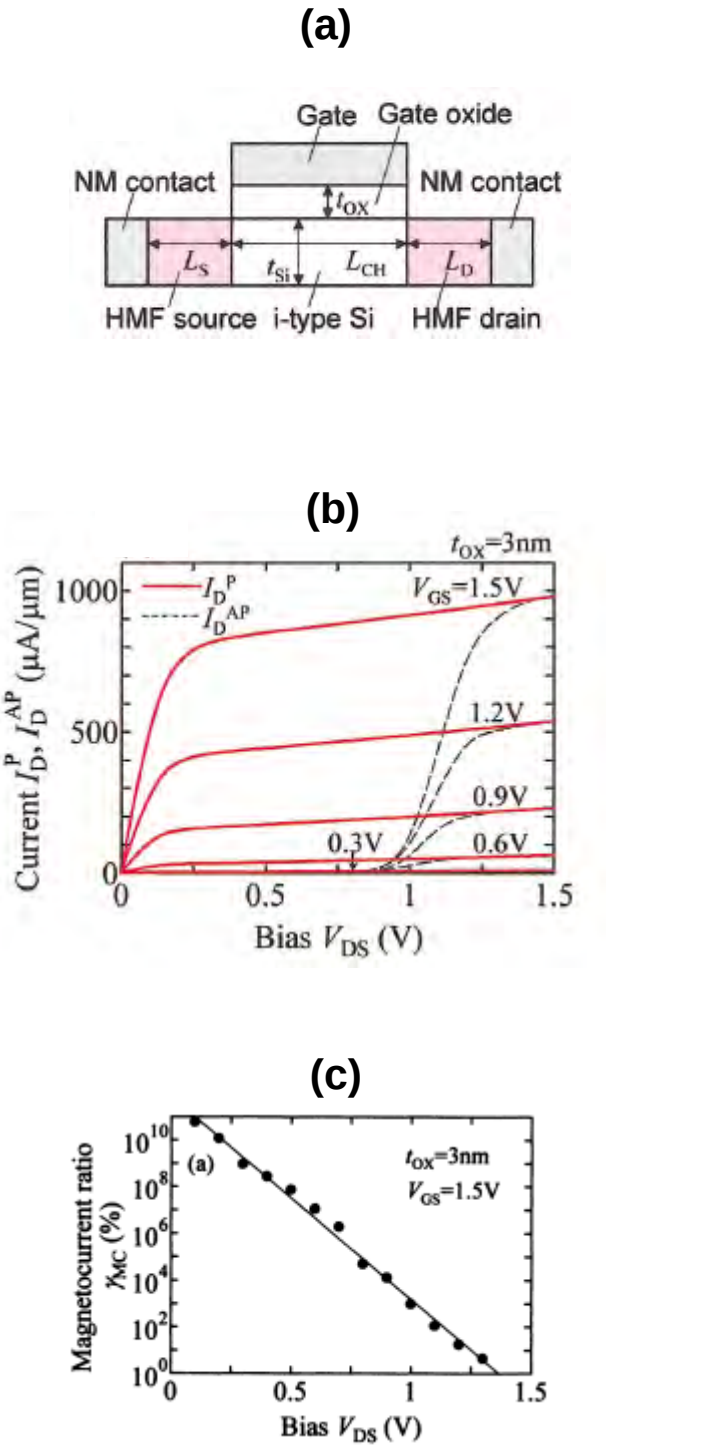


Fig. 2.4. (a) Device structure of Spin MOSFET. (b) Output characteristics of the spin MOSFET. The drain currents I_D^P (solid curves) and I_D^{AP} (dashed curves) in the parallel and antiparallel magnetic configurations, respectively, are plotted as a function of V_{DS} , where V_{GS} is varied from 0.3 to 1.5 V. (c) Magnetocurrent ratio as a function of V_{DS} at V_{GS} of 1.5 V [61].

In order to realize spintransistors, it is essential that efficient spin injection/detection for their semiconductor channel is established [61]. However, this is not so easy in practice owing to several problems related to the ferromagnet/semiconductor interfaces, such as interfacial layer formation, Fermi level pinning, and conductivity mismatch problems [62-64]. Although feasible technologies for these interface problems have been explored so far, definitive solutions for them are still at the stage of searching. Y. Shuto et. al previously proposed a new circuit approach using an ordinary MOSFET and magnetic tunnel junction (MTJ) for reproducing functions of spintransistors, referred to as a pseudo-spin-MOSFET (PSMOSFET) [65]. Recently the MTJ technology has dramatically progressed due to the development of MgO tunnel barriers. Furthermore, half-metallic ferromagnet electrodes using full-Heusler alloys would also have a great impact on the MTJ technology. In these situations, recently developed MTJs can exhibit a high tunneling magnetoresistance (TMR) ratio over 100 % at room temperature (RT) [66].

Figure 2.5(a) and (b) show the circuit configuration of the proposed PS-MOSFET and schematic side view of the fabricated PS-MOSFET, respectively. Figure 2.6(a) shows the output characteristics of the fabricated PS-MOSFET. The drain currents are plotted as a function of drain bias (V_D) swept from 0 to 2 V, where the gate bias (V_G) varies from -2 to 3V in steps of 1V. Solid curves (I_{DP}) and broken curves (I_D^{AP}) in the figure show the drain currents in the parallel and antiparallel magnetization configurations, respectively. The depletion-type field-effect transistor behavior was clearly observed, as described previously. I_D^P was higher than I_D^{AP} over the entire linear and saturation regions, indicating that the PS-MOSFET successfully operated as a spin-transistor. Figure 2.6(b) shows the drain current of the PS-MOSFET as a function of magnetic field at RT, where V_D = 0.1 V and V_G = 2 V. The magnetocurrent ratio defined as $(I_D^P - I_D^{AP})/I_D^{AP}$ was 38.4 %.

These results indicate that PS-MOSFET would be the most promising spin transistor that can be achieved by utilizing the MTJ technology.

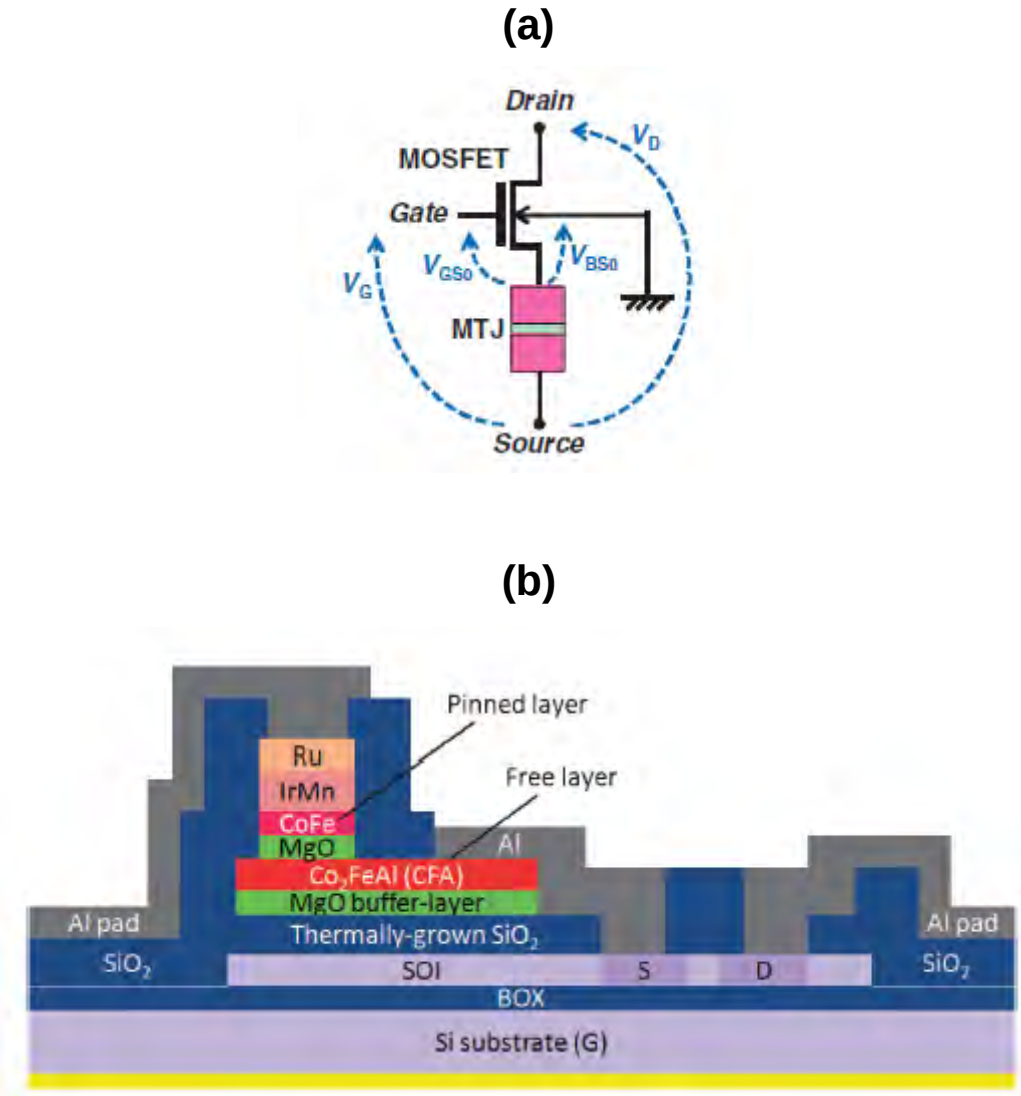


Fig. 2.5. (a) Circuit configuration of the proposed pseudo-spin-MOSFET (PS-MOSFET). (b) Schematic side view of the fabricated PS-MOSFET [65].

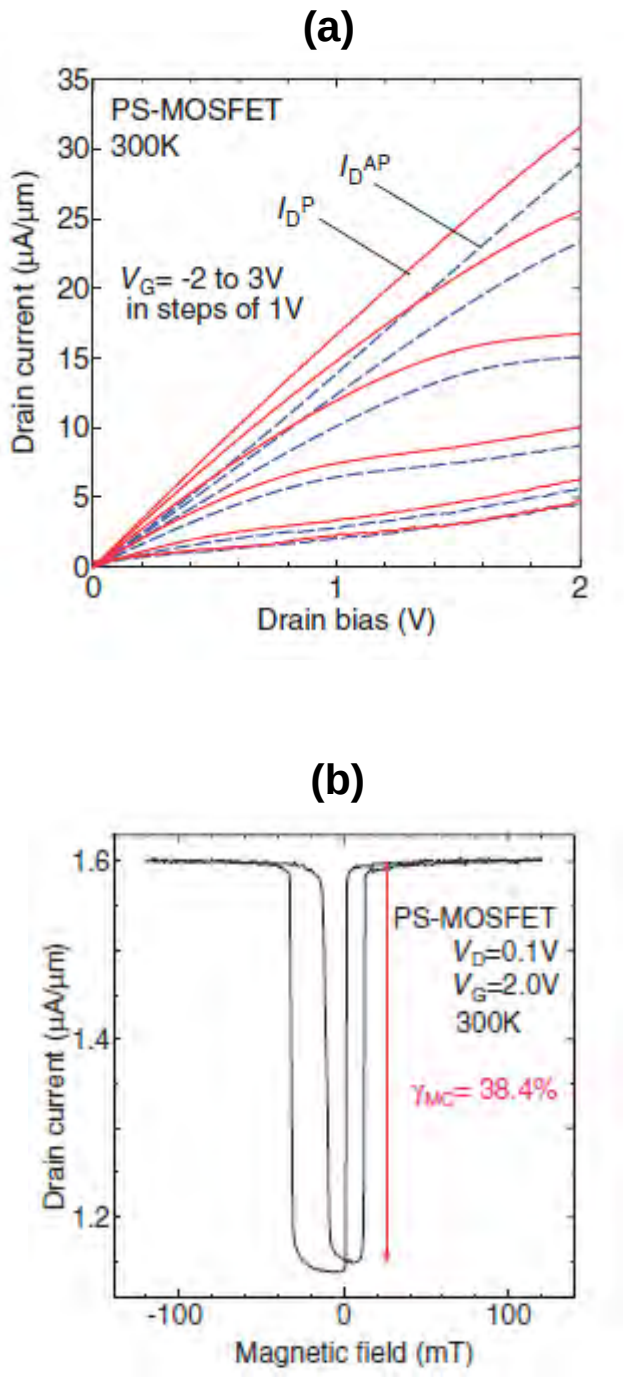


Fig. 2.6. (a) Output characteristics of the fabricated PS-MOSFET at RT. The drain currents are plotted as a function of drain bias V_D, where gate bias V_G varies from -2 to 3 V in steps of 1 V. Solid curves (I_D^P) and broken curves (I_D^{AP}) show the drain currents in the parallel and antiparallel magnetization configurations, respectively. (b) Drain current as a function of magnetic field at RT, measured with V_D = 0.1 V and V_G = 2 V [65].

2.4 Magnetoresistive Effects in Nonmagnetic Materials

A magnetic field sensor is an entrance transducer that converts a magnetic field into an electronic signal. Magnetoresistance (MR) effects in ferromagnetic tunnel junctions have generated considerable interest due to their application in magnetic data storage and memory devices [67, 68]. Additionally, tunnel magnetoresistance (TMR) ratio of around 200 % was experimentally realized at room temperature in the Fe(Co)/MgO/Fe(Co) magnetic tunnel junctions [66, 69]. Thus, the application of magnetic tunnel junctions has become a key issue in the development of spintronics. Recently, large TMR of 1056% at room temperature has been realized in MgO based double barrier magnetic tunnel junction [70]. Moreover, spin-transistors using an ordinary metal-oxide-semiconductor field-effect-transistor (MOSFET) and magnetic tunnel junctions are proposed [65].

In contrast, research on magnetotransport of semiconductors without using magnetic materials is a field of increasing interest. Recently, nonmagnetic materials such as InSb exhibit geometric MR, which are orders of magnitude larger than the physical MR of other materials [71]. Furthermore, large positive MR effects were also reported in several nonmagnetic semiconductors such as Au/semi-insulating GaAs Schottky diode [72] and B-doped Si [73] MnSb granular films [74].

Figure 2.7(a) shows the schematic illustration of the Au/semi-insulating GaAs Schottky diode [72]. Figure 2.7(b) shows the *I–V* curves measured under various perpendicular magnetic fields. When a small magnetic field was applied, the threshold voltages for the avalanche breakdown shift to a higher voltage. A nearly linear relationship between threshold voltages and the applied magnetic field can be deduced from the measurements. Also the jumps of current due to avalanche breakdown became less and less steep with increasing magnetic field, as clearly reflected in the curves of 0.03 and 0.1 T. Figure 2.7(c) shows the measured current-magnetic field curve under 33 V and its corresponding MR ratio curves.

The MR ratio is defined as $(R(B)/R(0) - 1) \times 100$ %, Here, R (0) and R (B) are the resistances of the sample at 0 T and B T, respectively. The device was operated in high-current avalanche breakdown state because the operated voltage is higher than the threshold voltage. As shown in the figure, with the increasing magnetic fields the current continuously decreases. A sharp decrease of current occurs at around 0.2 T, above 0.2 T the current is largely depressed. The corresponding MR ratio also shows a quick increase before the 0.2 T. MR ratio reaches 3 000% at 0.2 T. Then MR ratio shows a continuous increase, reaching 100 000% at 0.8 T. It is considered that these behaviors are caused by a magnetic-field-controlled impact ionization of carriers. It is known that the large magnetoresistance is caused by impact ionization of carriers. At zero magnetic fields, for voltages greater than the threshold voltage the sample is in high current state, indicating a significant concentration of hot electrons with energies above the mobility edge. The application of a magnetic field increases the density of states at the bottom of the lowest Landau level, causing electrons to occupy states with lower and lower energy. Accordingly the current decreases since fewer and fewer electrons can take part in the impact ionization process. Impact ionization vanishes when the concentration of electrons thermally activated above the mobility edge is insufficient to trigger the avalanche, these results in a quick decrease of current and disables the breakdown. That’s why the large MR effect occurred easily in breakdown regime.

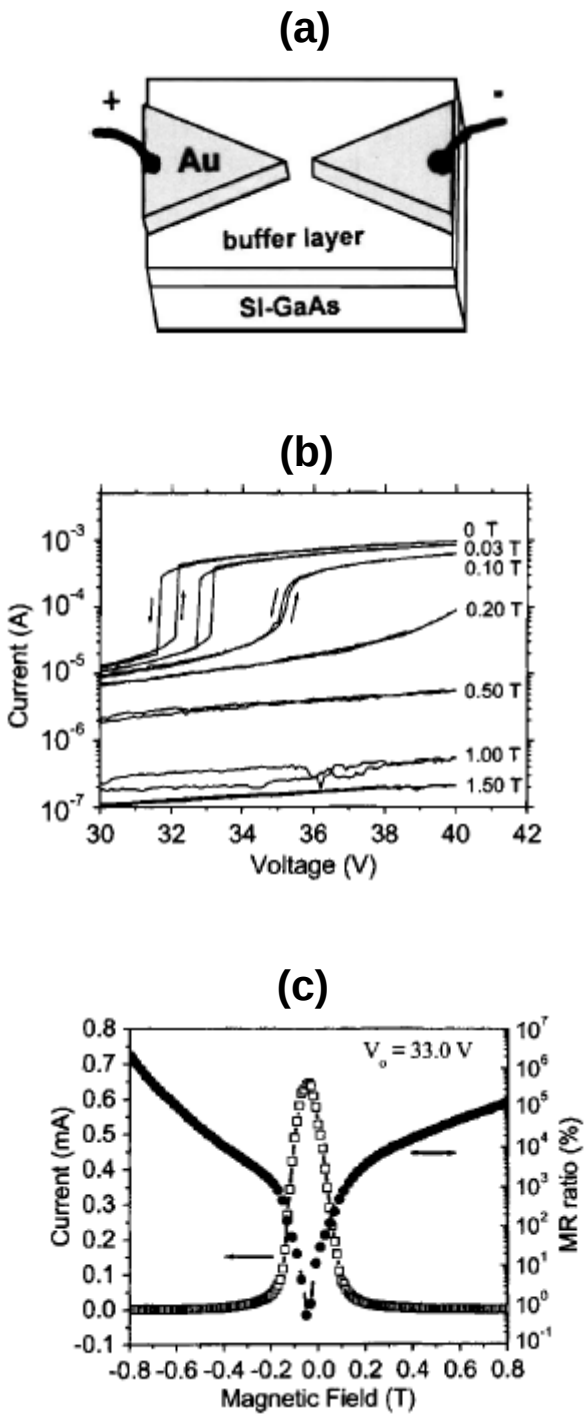


Fig. 2.7. (a) Schematic illustration of the Au/SI-GaAs Schottky diode used for transport measurements. The two Au electrodes were fabricated on the semi-insulating GaAs by photolithography using the wet-etching method. The gap size is 2 mm. (b) RT current–voltage characteristic curve of Au/SI GaAs devices measured under various applied magnetic fields. (c) Current–magnetic field relationship (left axis) and corresponding magnetoresistive ratio curves (right axis) measured at operating voltage of 33 V [72].

In 2009, it has been found that P-doped Si shows a large positive MR between 0 and 3 T of more than 1,000 % at 300 K and 10,000 % at 25 K [75]. Figure 2.8(a) shows the sketch of the P-doped Si substrate in the experiment performed by Delmo et. al. [75]. Figure 2.8(b) shows the *I–V* characteristics of the device made of the intrinsic silicon (i-Si) ($n = 1.78 \times 10^{12}$ cm^{-3} and μ = 1,300 $cm^2/V \cdot s$ at 300 K). The photo of the device is shown in the inset of the figure. Although the *I–V* characteristics at 300 K show ohmic behaviors at low bias voltages, the behaviour changes for V = 50 V, signaling the space-charge effect. Figure 2.8(c) shows the large positive MR observed for V = 50 V and, for comparison, the usual small, quadratic MR observed at V = 25 and 50 V. This phenomenon can be explained by the quasi-neutrality breaking of the space-charge effect, where insufficient charge is present to compensate the electrons injected into the device [76, 77].

In this brake down regime the space-charge effect is considered to be important because the injected carrier density (n_{inj}) is larger than the equilibrium carrier density of the silicon (n_{eq}). The n_{inj} is expressed as $JL/q\mu V$, where J is the current density, L is the electrode spacing, q is the electron charge, μ is the mobility, and V is the bias voltage. Actually, by using the other device parameters (L = 0.1 mm, μ = 1.96 $m^2/V \cdot s$, and $n_{eq} = 2.73 \times 10^9$ cm^{-3} at 25 K), Delmo et. al. obtained n_{inj}/n_{eq} = 1.7 for I = 0.2 mA and V = 8.56 V, which clearly demonstrates the significance of the space-charge effect.

Consider a piece of material that has non-zero conductivity and has two ohmic contacts at both sides. An electric current is injected into the material from one of the contacts and extracted from the other as a finite voltage difference is maintained between them. Because there are usually many positive and negative charges that are equal in number in the material, the injected small amount of charge is immediately compensated by the background charges and by the charges from the extraction contact to achieve quasi-neutrality, which results in the uniform electric field in the material [78]. The conventional free electron model describes that

the electrons have constant drift velocity and the external magnetic field perpendicular to the current does not affect the two-terminal resistance between the contacts [78]. When more electrons are injected to break the quasineutrality, the accumulation of the injected electrons, namely the space-charge effect [79-82] occurs to generate an electric field unevenly distributed inside the material. The motion of the electrons is no longer trivial; the absence of the compensating charges makes the electrons correlate with each other via the unscreened Coulomb interaction such that their velocity becomes dependent on the local electric field and hence on their trajectory. The Hall field that is generated by the carrier motion in the magnetic field in the broken quasi-neutrality is expected to be very different from the simple Hall field that the conventional free electron model describes. Although it is naively expected that in this regime the modification of the electron trajectory by the magnetic field may result in an unusual electron transport such a possibility has never been explored, it have been found large magnetoresistance in silicon recently.

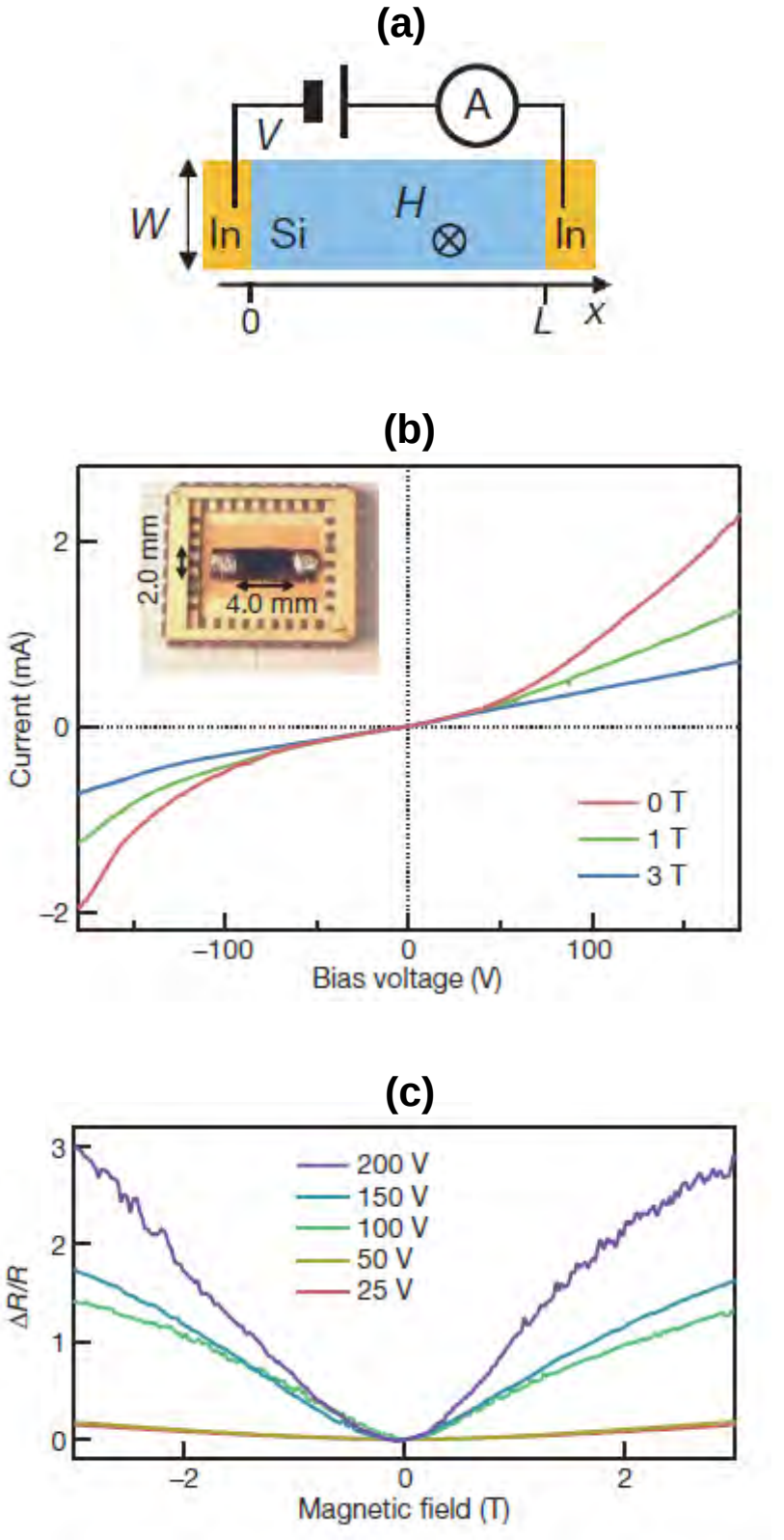


Fig. 2.8. (a) Sketch of the device. L is the distance between the contacts and W is their width. The magnetic field, H, is applied perpendicular to the current direction. (b) *I–V* characteristics of the In/i-Si/In device in the magnetic field of 0, 1 and 3 T. Inset, photo of the In/i-Si/In device with device dimensions. Its thickness is 380 mm. (c) MR for various bias voltages [75].

The observation of a large MR in Si, based on this phenomenon, is an important milestone towards new spintronics applications. Actually, for sensing application, there is a Corbino disk which consists of InSb with high electron mobility of 78000 $cm^2/V \cdot s$ [83]. With the aim towards its application to electronic devices, the MR of a two-dimensional electron gas in a disordered Si (metal-oxide-semiconductor field-effect-transistor (Si-MOSFET)) system is measured at a magnetic field of 40 T [84]. In this device, the MR of 100 % was obtained since the MR was considered as a result of modified scattering due to screening and density of states modifications caused by the spin polarization of the two-dimensional electron gas [85]. Furthermore, Si-MOSFET structures exhibit a positive MR of about 18 % at room temperature with a magnetic field of 9 T, due to the presence of high-mobility electrons in the Si inversion layer [86]. Moreover, MR measurements were performed on n-type Si MOS field-effect transistors (FET), and this device exhibits 12 % of MR at 300 K under the magnetic field of 10 T [87].

Recently, C. Ciccarelli et. al studied the MR of a Si MOSFET at the break-down regime when a magnetic field is applied perpendicular to the plane of the device at 4.2 K [88]. The different nature of the MR for gate voltages above and below the threshold is highlighted in Fig. 2.9(a). The MR is shown as $(R(B)/R(0) - 1) \times 100$ %, with the magnetic field applied perpendicularly to the plane of the device, at high V_{SD}. For V_G above the threshold gate voltage (V_G^{th} = 0.3 V) the MR saturates at high fields. Furthermore, C. Ciccarelli et. al also compare the break-down source-drain voltage at zero and large magnetic field up to 10 T. As it becomes obvious in Fig. 2.9(b), the MR at high V_{SD} values is caused by the suppression of the break-down current and this suggests a strong entanglement between the MR and the mechanisms that lead to the break-down. Moreover, the MR in devices with different channel dimensions is studied. It has been previously suggested by Delmo et al.[75] that the large MR can also be obtained in smaller devices, if the high mobility and low equilibrium carrier

concentration conditions are satisfied, as long as the electrons remain correlated. The MR curves of two smaller devices with channel dimensions of 5×5 μm^2 and 5000×800 nm^2, shown in Fig. 2.9(c). The MR is two orders of magnitude lower in the smaller devices, even though the value of the effective electric field applied between the source and the drain is two orders of magnitude larger. By reducing only the channel width of the device from 5 μm to 800 nm, the MR further drops by a factor of two at 10 T. These results indicate that the channel dimensions are important for the MR effects in MOSFETs.

Finally, figure 2.10(a) shows the comparison of these MR effects in various materials at 300 K. Furthermore, the MR of these nonmagnetic materials and devices are plotted in Fig. 2.10(b).

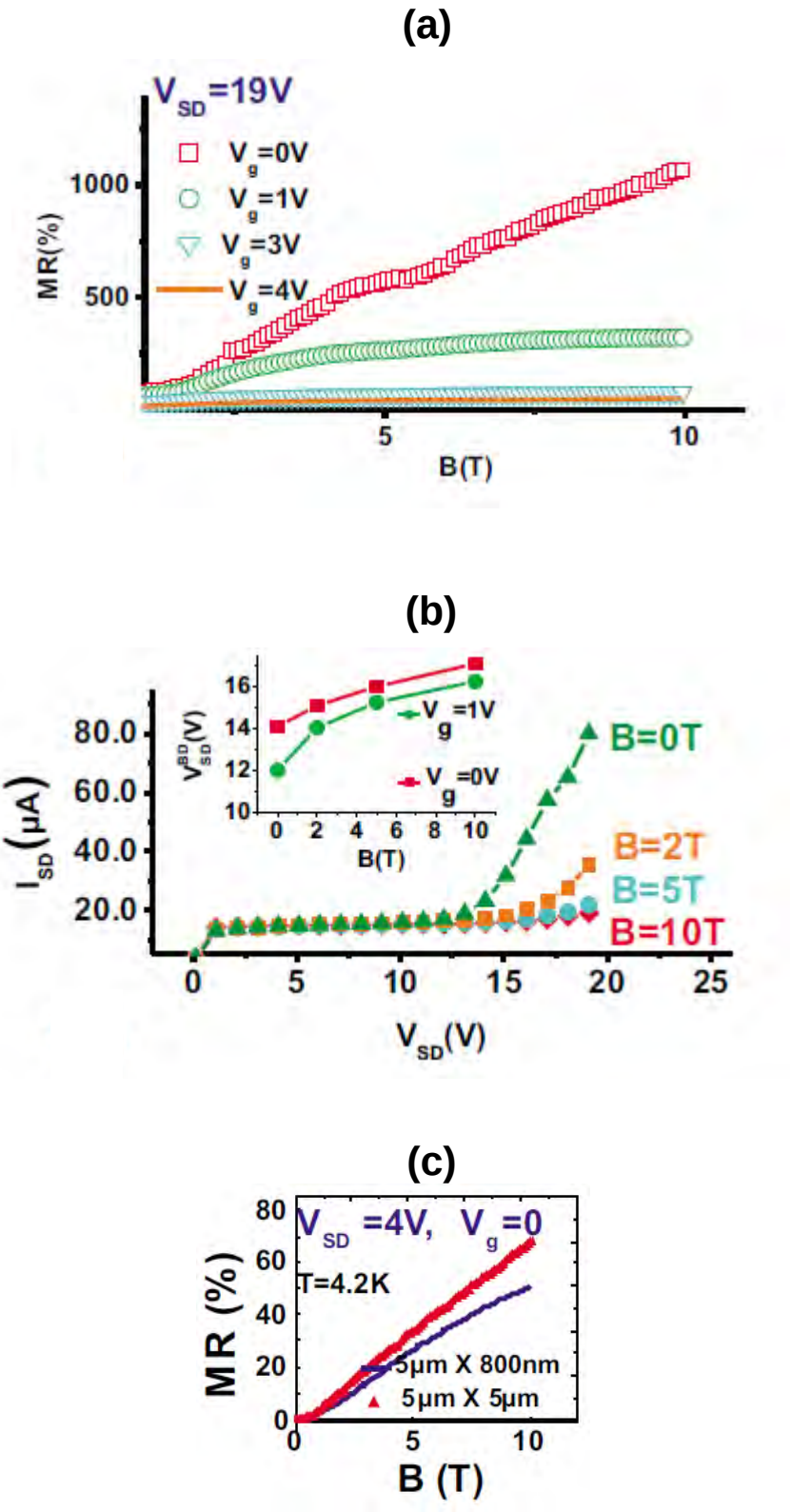


Fig. 2.9. (a) MR of the MOSFET channel at different values of the gate voltage. (b) Current vs source to drain bias graphs of the MOSFET for $V_G = 1$ V at different values of the magnetic field. Inset: dependence of the break-down source to drain bias with B for $V_G = 1$ V (circles) and $V_G = 0$ V (squares). (c) MR vs B curves are measured at $V_G = 0$ V in the device dimensions of 5×5 μm^2 and 5000×800 nm^2 [88].

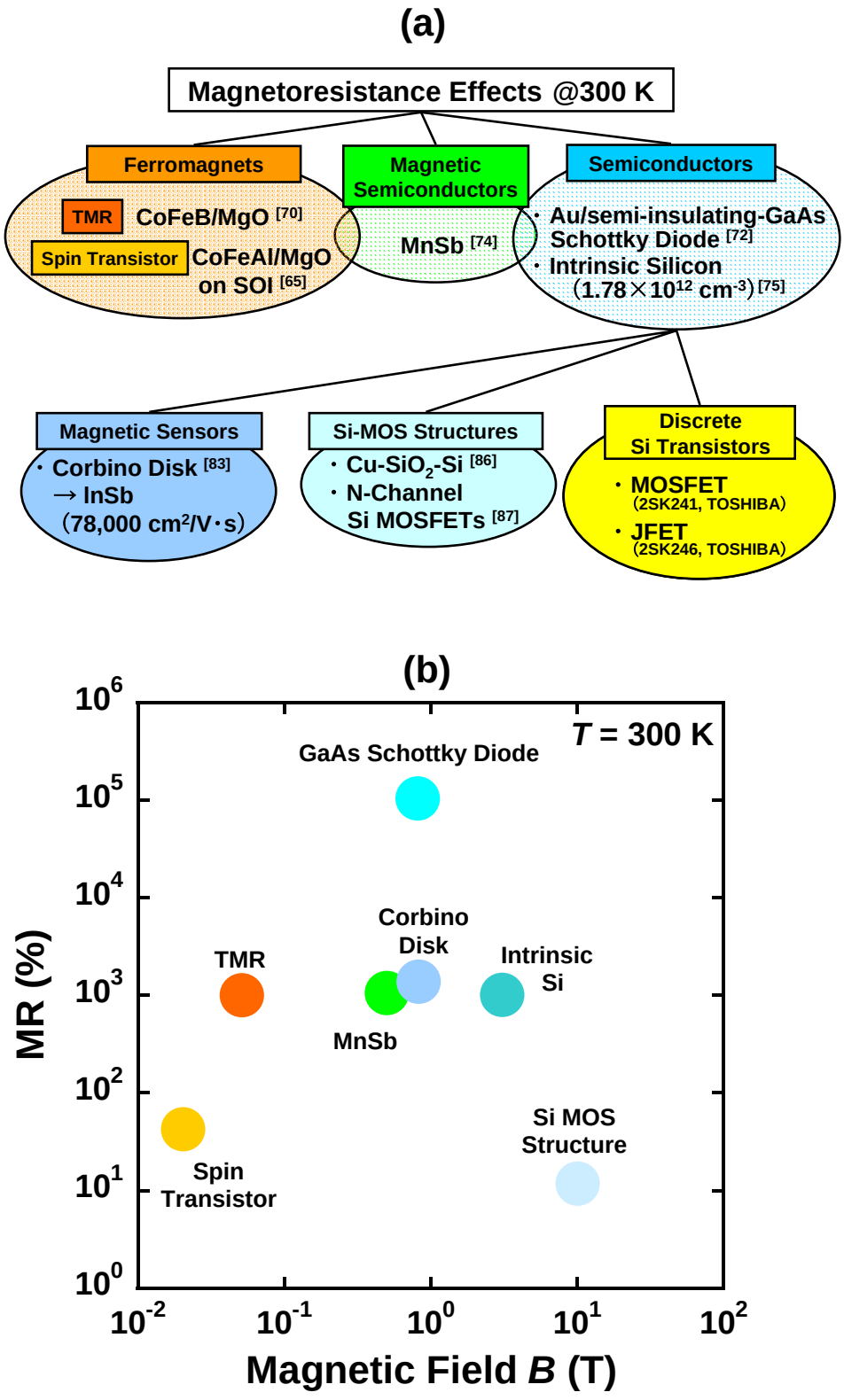


Fig. 2.10. (a) Comparison of these MR effects in various materials and devices at room temperature (b) MR of various materials and devices in (a).

2.4.1 Geometrical Magnetoresistive Effects

Here, the geometrical MR effect of MOSFET is described. Figure 2.11 shows the schematic of MOSFET structure. In the presence of a magnetic field aligned perpendicular to the current flow plane, the conductivities of the two-dimensional electron gas are expressed as follows,

$$\begin{aligned} j_x &= \sigma_{xx} E_x + \sigma_{xy} E_y, \\ j_y &= -\sigma_{xy} E_x + \sigma_{xx} E_y, \end{aligned} \tag{2.1}$$

where E_x and E_y are the electric fields in the x and y planes, respectively [89]. Furthermore, σ_{xx} and σ_{xy}, which are the components of the conductivity tensor, are also described as follows [90],

$$\begin{aligned} \sigma_{xx} &= \sigma_0 /(1+\mu^2 B^2), \\ \sigma_{xy} &= \sigma_0 \mu B /(1+\mu^2 B^2). \end{aligned} \tag{2.2}$$

where B is the magnetic field, μ is the electron mobility and $\sigma_0 = n_s e\mu$ with n_s and e being the sheet carrier concentration and charge, respectively. In the case of a very short and wide device ($L \ll W$, where L is the length in the direction of the current flow and W is the width of the device), the Hall voltage is short circuited by long current-supplying contacts, resulting in

$$E_y = 0, \tag{2.3}$$

then, the current density in the x direction at the magnetic field B is expressed as

$$j_x = \sigma_{xx} E_x = \sigma_0 /(1+\mu^2 B^2) \cdot E_x. \tag{2.4}$$

Additionally, the resistivity ρ_0 (0) at the magnetic field of 0 T is defined as

$$\rho_0(0) = 1/\sigma_0. \tag{2.5}$$

Therefore, the resistivity ρ_0 (B) in the presence of the magnetic field B is expressed as

$$\rho_0(B) = \rho_0(0) \cdot (1+\mu^2 B^2). \tag{2.6}$$

Finally, the MR induced by a geometrical effect (MR_{geo}) is described as

$$MR_{geo}(\%) = \frac{R(B) - R(0)}{R(0)} \times 100 = \frac{\rho_0(B) - \rho_0(0)}{\rho_0(0)} \times 100 = \mu^2 B^2 \times 100. \qquad (2.7)$$

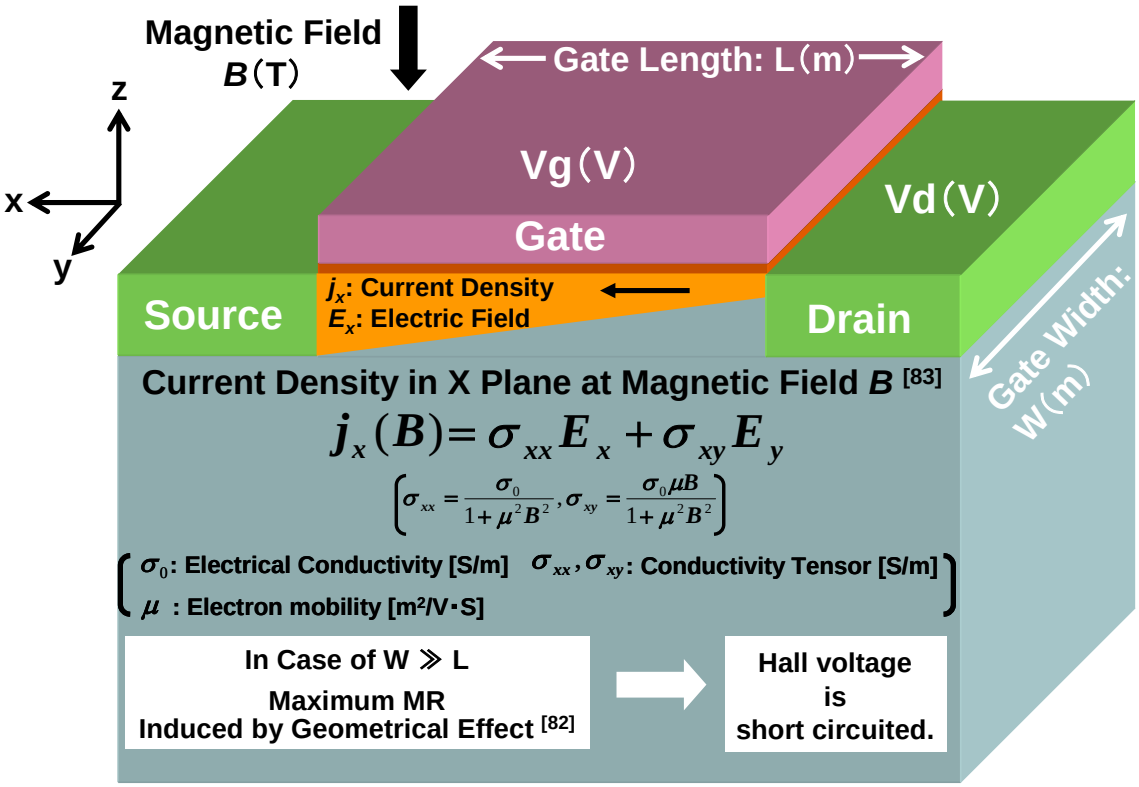


Fig. 2.11. Geometrical MR effect of MOSFET structure.

On the other hand, motion equation of electron in the magnetic field at the steady state is expressed as follows,

$$\begin{aligned} qE_x - \frac{m}{\tau_x} + qB\upsilon_y = 0, \\ qE_y - \frac{m}{\tau_x} - qB\upsilon_x = 0, \end{aligned} \tag{2.8}$$

where q is the electron charge, m is the electron effective mass,τ is relaxation time, and ν is the velocity of electron. Here, the electron mobility μ is described as

$$\begin{aligned} \mu_x = \frac{q\tau_x}{m}, \\ \mu_y = \frac{q\tau_y}{m}. \end{aligned} \tag{2.9}$$

Furthermore, the current density J is defined as

$$\begin{aligned} J_x = qn\upsilon_x, \\ J_y = qn\upsilon_y, \end{aligned} \tag{2.10}$$

where n is carrier concentration of electron. In the case of $L \gg W$, the Hall voltage V_H is not short circuited ($E_y \neq 0$). Therefore, current density J_x in x component is expressed as

$$J_x = \frac{\sigma_x (E_x + \mu_x B \frac{V_H}{W})}{1 + \mu_x \mu_y B^2}, \tag{2.11}$$

since σ_x is described as $nq\mu_x$. Here, the conductivity of x direction σ_x in the magnetic field is expressed as $\sigma_x(B)$, then $\sigma_x(B)$ is represented as

$$\sigma_x(B) = \frac{\sigma_x (1 + \mu_x B \frac{V_H \cdot L}{W \cdot V_D})}{1 + \mu_x \mu_y B^2}, \tag{2.12}$$

where the Ex is V_D/L.

Here the conductance of MOSFET as a function of x in the magnetic field is described as $Gx(B)$. The $Gx(B)$ is given by

$$G_x(B) = \left[qN_0\mu_x + \left\{C_i(V_G - V(x)) \cdot \mu_x\right\}\right] \frac{1 + \mu_x B \frac{V_H \cdot L}{W \cdot V_D}}{1 + \mu_x \mu_y B^2} \cdot \frac{W}{dx}, \quad (2.13)$$

where the gradual-channel approximation is applied [91].The gradual-channel approximation requires that longitude field be much smaller than the transverse field. This implies that V(x) is a slowly varying function such that a simple one-dimensional approximation can be used. Then, the drain current $I_D(B)$ of MOSFET in magnetic field is given by

$$I_D(B) = G_x(B)dV = \left[qN_0\mu_x + \left\{C_i(V_G - V(x)) \cdot \mu_x\right\}\right] \frac{1 + \mu_x B \frac{V_H \cdot L}{W \cdot V_D}}{1 + \mu_x \mu_y B^2} \cdot W \cdot \frac{dV}{dx}, \quad (2.14)$$

Integrating Eq. (2.14) from x = 0 to L yield,

$$\int_0^L I_D(B)dx = \int_0^L \left[qN_0\mu_x + \left\{C_i(V_G - V(x)) \cdot \mu_x\right\}\right] \frac{1 + \mu_x B \frac{V_H \cdot L}{W \cdot V_D}}{1 + \mu_x \mu_y B^2} \cdot W \cdot \frac{dV}{dx} \cdot dx, \quad (2.15)$$

then,

$$I_D(B) \cdot L = \int_0^{V_D} \left[qN_0\mu_x + \left\{C_i(V_G - V(x)) \cdot \mu_x\right\}\right] \frac{1 + \mu_x B \frac{V_H \cdot L}{W \cdot V_D}}{1 + \mu_x \mu_y B^2} \cdot W \cdot dV. \quad (2.16)$$

Here, the drain current in the magnetic filed is expressed as

$$I_D(B) = \frac{1 + \mu_x B \frac{V_H \cdot L}{W \cdot V_D}}{1 + \mu_x \mu_y B^2} \cdot \frac{WC_i\mu_x}{L}\left[(V_G - V_T)V_D - \frac{{V_D}^2}{2}\right], \quad (2.17)$$

where qN_0 is equal to $-C_iV_T$, the gate capacitance, drain voltage, and gate voltage are expressed as the symbol of C_i, V_D, and V_T, respectively.

Furthermore, the current density I_D (0) of MOSFET in x direction is expressed as

$$I_D(0) = \frac{WC_i\mu_x}{L}\left[(V_G - V_T)V_D - \frac{{V_D}^2}{2}\right], \quad (2.18)$$

Therefore, when electron mobility μ is $\mu_x = \mu_y$, MR effect of MOSFET in the case of $L \gg W$ ($E_y \neq 0$) is described as

$$MR_{E_y \neq 0}(\%) = \frac{I_D - I_D(B)}{I_D(B)} \times 100 = \frac{\mu^2 B^2 - \mu B \dfrac{V_H \cdot L}{W \cdot V_D}}{1 + \mu B \dfrac{V_H \cdot L}{W \cdot V_D}} \times 100(\%)$$

(2.19)

Figure 2.12(a) and (b) shows the theoretical prospect of drain current and MR as a function of drain voltage based on Eq. (2.19) at the case of $V_H \neq 0$ and $V_H = 0$, respectively. Figure 2.12(c) shows the MR as a function of Hall voltage V_H. In theses cases, the mass of electron m_0 is considered to be $m_0 = m_l = m_t$, where m_l and m_t are the transverse and longitudinal electron effective masses, respectively. Here, the MR dependence of MOSFET on magnetic filed with $m_t = 0.19m_0$ and $m_l = 0.98m_0$ [92] are shown in Fig. 2.13. These results indicate that the MR of MOSFET is strongly affected by the mobility and effective mass of electron.

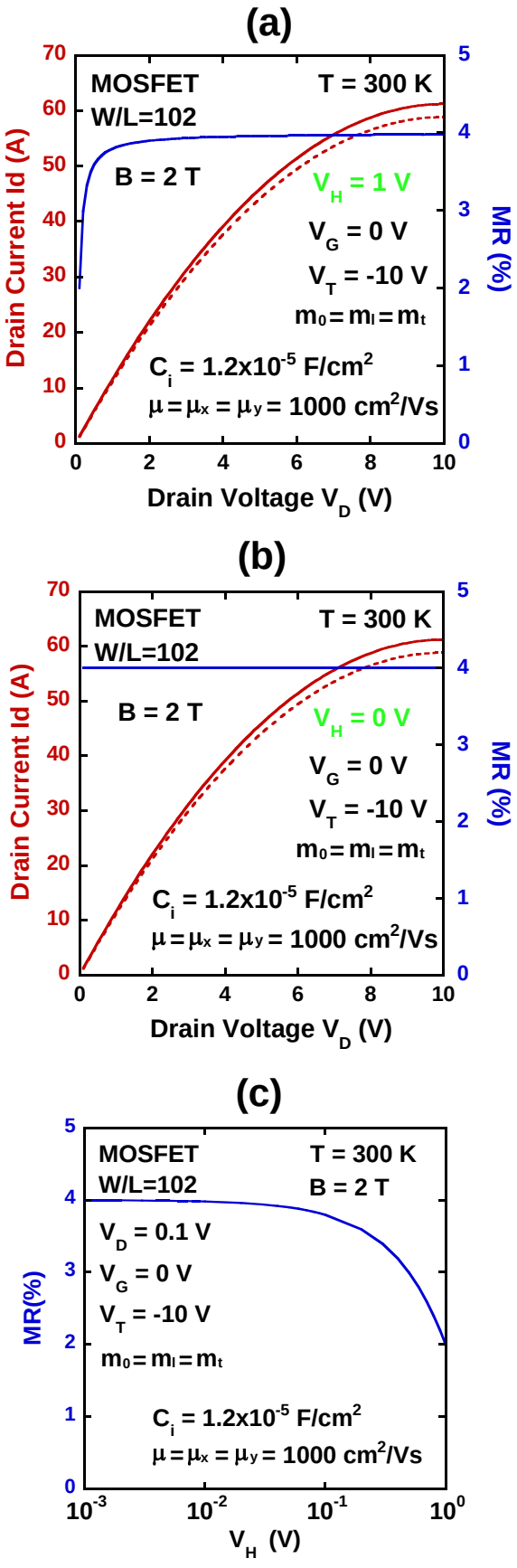


Fig. 2.12. Theoretical prospect of drain current and MR in MOSFET (W/L=102) as a function of drain voltage at the case of (a) V_H = 1 V and (b) V_H = 0, respectively. Magnetic field of 2 T is applied to the MOSFET. (c) MR as a function of Hall voltage V_H.

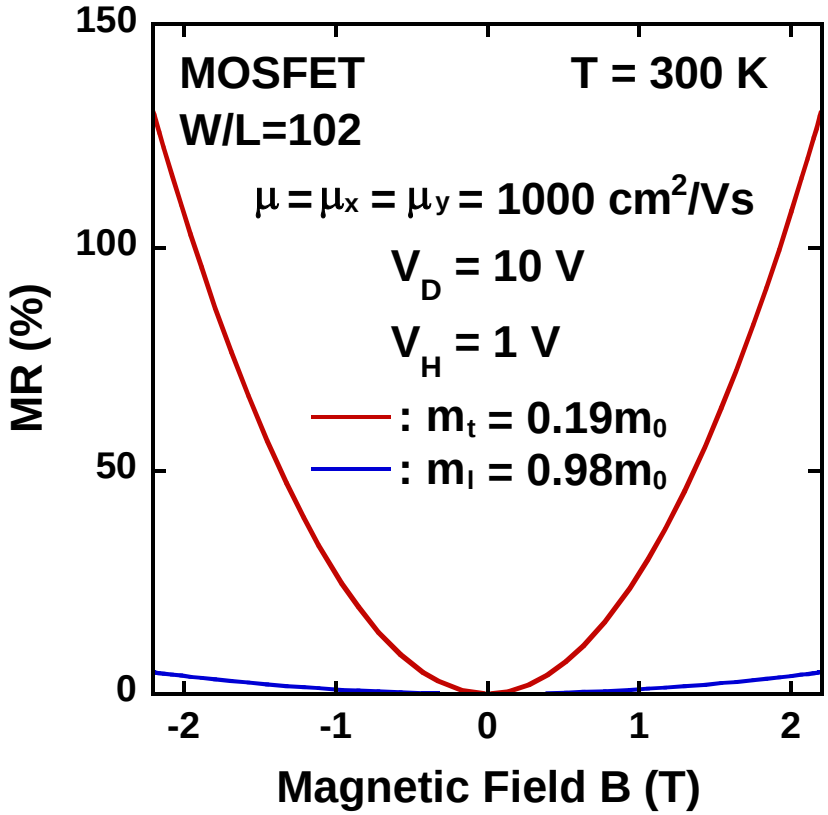


Fig. 2.13. MR dependence of MOSFET on magnetic filed B with the longitudinal effective mass of $m_l = 0.98m_0$ and $m_t = 0.19m_0$.

2.4.2 Transverse Magnetoresistive Effects

Finally, transverse MR is mentioned in this chapter. Transverse MR is one of the galvanomagnetic effects, in which a magnetic field perpendicular to an electric current gives rise to an electrical potential change in the direction of the current. The conductivity tensor of electron σ_e and hole σ_h in the magnetic field are expressed as follows,

$$\sigma_e = \frac{\sigma_e^0}{1+\omega_{ce}^2\tau_e^2}\begin{pmatrix} 1 & -\omega_{ce}\tau_e & 0 \\ \omega_{ce}\tau_e & 1 & 0 \\ 0 & 0 & 1+\omega_{ce}^2\tau_e^2 \end{pmatrix} \tag{2.20}$$

$$\sigma_h = \frac{\sigma_h^0}{1+\omega_{ch}^2\tau_h^2}\begin{pmatrix} 1 & \omega_{ch}\tau_h & 0 \\ -\omega_{ch}\tau_h & 1 & 0 \\ 0 & 0 & 1+\omega_{ch}^2\tau_h^2 \end{pmatrix} \tag{2.21}$$

where, ω_{ce} and ω_{ch} are cyclotron resonance of electron and hole, respectively. The τ_e and τ_h are also relaxation time of electron and hole, respectively. In this case, current density J_x and J_x become to be expressed as fpllows.

$$J_x = \left(\frac{\sigma_e^0}{1+\omega_{ce}^2\tau_e^2} + \frac{\sigma_h^0}{1+\omega_{ch}^2\tau_h^2}\right)E_x - \left(\frac{\sigma_e^0\omega_{ce}\tau_e}{1+\omega_{ce}^2\tau_e^2} - \frac{\sigma_h^0\omega_{ch}\tau_h}{1+\omega_{ch}^2\tau_h^2}\right)E_y \tag{2.22}$$

$$J_y = \left(\frac{\sigma_e^0\omega_{ce}\tau_e}{1+\omega_{ce}^2\tau_e^2} - \frac{\sigma_h^0\omega_{ch}\tau_h}{1+\omega_{ch}^2\tau_h^2}\right)E_x + \left(\frac{\sigma_e^0}{1+\omega_{ce}^2\tau_e^2} + \frac{\sigma_h^0}{1+\omega_{ch}^2\tau_h^2}\right)E_y \tag{2.23}$$

Here, conductivity tensor, mobility, and cyclotron resonance are also described as following equation,

$$\sigma_e^0 = \frac{nq^2\tau_e}{m_e} = nq\mu_e, \mu_e = \frac{q\tau_e}{m_e}, \omega_{ce} = \frac{qB}{m_e c} \tag{2.24}$$

$$\sigma_h^0 = \frac{nq^2\tau_h}{m_h} = nq\mu_h, \mu_h = \frac{q\tau_h}{m_h}, \omega_{ce} = \frac{qB}{m_h c} \tag{2.25}$$

where, n, q, B are the carrier concentration, electron charge, and magnetic field. Furthermore, c is 3.0×10^{10}. Therefore, current densities are given by

$$J_x = \left(\frac{nq\mu_e c^2}{c^2 + B^2\mu_e^2} + \frac{pq\mu_h c^2}{c^2 + B^2\mu_h^2} \right) E_x - \left(\frac{nqB\mu_e^2 c}{c^2 + B^2\mu_e^2} - \frac{pqB\mu_h^2 c}{c^2 + B^2\mu_h^2} \right) E_y \tag{2.26}$$

$$J_y = \left(\frac{nqB\mu_e^2 c}{c^2 + B^2\mu_e^2} - \frac{pqB\mu_h^2 c}{c^2 + B^2\mu_h^2} \right) E_x + \left(\frac{nq\mu_e c^2}{c^2 + B^2\mu_e^2} + \frac{pq\mu_h c^2}{c^2 + B^2\mu_h^2} \right) E_y \tag{2.27}$$

When J_y is 0, E_y is expressed as

$$E_y = -\frac{\frac{nqB\mu_e^2 c}{c^2 + B^2\mu_e^2} - \frac{pqB\mu_h^2 c}{c^2 + B^2\mu_h^2}}{\frac{nq\mu_e c^2}{c^2 + B^2\mu_e^2} + \frac{pq\mu_h c^2}{c^2 + B^2\mu_h^2}} E_x \tag{2.28}$$

Therefore, current density J_x is descrived as follows

$$J_x = \left(\frac{nq\mu_e c^2}{c^2 + B^2\mu_e^2} + \frac{pq\mu_h c^2}{c^2 + B^2\mu_h^2} \right) E_x + \left(\frac{nqB\mu_e^2 c}{c^2 + B^2\mu_e^2} - \frac{pqB\mu_h^2 c}{c^2 + B^2\mu_h^2} \right) \frac{\frac{nqB\mu_e^2 c}{c^2 + B^2\mu_e^2} - \frac{pqB\mu_h^2 c}{c^2 + B^2\mu_h^2}}{\frac{nq\mu_e c^2}{c^2 + B^2\mu_e^2} + \frac{pq\mu_h c^2}{c^2 + B^2\mu_h^2}} \tag{2.29}$$

Here, resistivity ρ_x in x direction at the magnetic field is given by

$$\rho_x(B) = \frac{E_x}{J_x} \tag{2.30}$$

Finally, the transverse MR in the x direction is expressed as following formura.

$$MR_{transverse}(\%) = \frac{\rho_x(B) - \rho_x(0)}{\rho_x(0)} \times 100 \tag{2.31}$$

Figure 2.14 shows the theoretical prospect of transverse MR based on Eq. (2.31) at the case of n-type Si substrate.

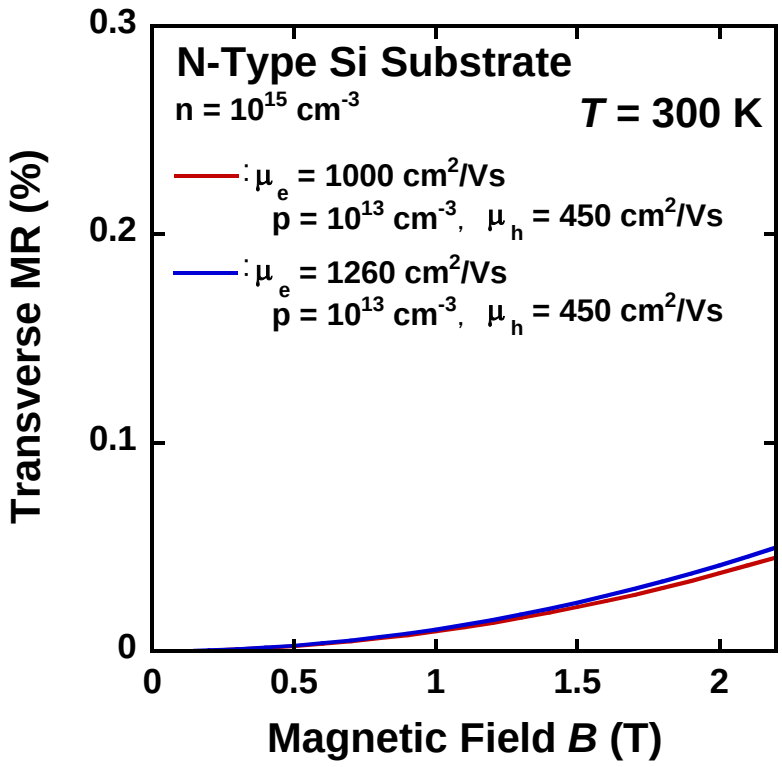


Fig. 2.14. Theoretical prospect of transverse MR based on Eq. (2.31) at the case of n-type Si substrate.

2.5 Summary

Recent discoveries of large magnetoresistance in non-magnetic semiconductors have gained much attention because the size of the effect is comparable to, or even larger than, that of magnetoresistance in magnetic systems. Conventional magnetoresistance in doped semiconductors is straightforwardly explained as the effect of the Lorentz force on the carrier motion, but the reported unusually large effects imply that the underlying mechanisms have not yet been fully explored. One of them is space charge effect and impact ionization of carriers.

Chapter 3

SPM Local Oxidation Lithography at Micro- and Nano-Scales

3.1 Introduction

Local oxidation nanolithography using scanning probe microscopy (SPM) has been widely used to produce nanometer-scale structures on the substrate surface [1]. This technique is recognized as possible nanofabrication tools for nanoelectronics applications such as single-electron transistors (SETs) [2, 3] and planar-type ferromagnetic tunnel junctions [4, 5]. In general, the feature size of the oxide is strongly affected by the size of the water meniscus [6], relative humidity [7], applied bias voltage [8], scanning speed of the SPM cantilever [8], and operation mode [9]. The advantages of SPM local oxidation are its operation in ambient air, the simple production of nanometer-scale structures, and fabrication without masks or lift-off processes. On the other hand, in terms of writing speed, conventional SPM local oxidation has a low throughput (defined as the oxide area divided by the writing time) of 0.027 $\mu m^2/s$ [10]. Thus, in view of applications for Si devices, it is considered that conventional SPM-based nanolithography is not suitable in terms of the fabrication throughput because nanometer-scale devices such as SETs are composed of submicrometer-scale current confinement structures and micrometer-scale device separation/isolation regions.

In order to investigate the key factors that control the growth of Si oxide, we have studied that SPM local oxidation at micro- and nano-scales. We perform a comparative study of the size dependence of the Si oxide wires on the Q-factor and the oscillation amplitude of the cantilever used in tapping mode operation. Additionally, we quantitatively explain the

size of the oxide controlled with tapping mode local oxidation using a model based on the oxidation ratio and the rate constant of the oxidation reaction.

3.2 SPM Local Oxidation Techniques

Nanometer-scale structures fabricated by using SPM local oxidation have been mainly controlled by applied bias voltage [8], scanning speed [8] and ambient humidity [7]. Figure 3.1 shows a schematic of local oxidation nanolithography process using tapping mode SPM. The reaction mechanism of the SPM local oxidation is considered to be the anodic oxidation. Since the local oxidation using SPM requires the field-induced formation of water meniscus between a conductive SPM tip and material surface, a negative bias voltage is applied to the SPM tip. Consequently, the water meniscus connects the SPM tip and the material surface and creates oxyanions (OH^-, O^-) from water molecules. These oxyanions act as reaction species in order to form the oxide. In this way, one can easily obtain the oxide wires with a feature size of around 10 nm, which suggests the spatial dimension of water meniscus [11, 12].

In contact mode SPM local oxidation, it has been reported that growth rate of the fabricated oxide in case of applying AC bias voltage to the SPM tip was larger than that of DC bias voltage [13]. This suggests that space charge (H^+) build-up within the fabricated oxide during the SPM local oxidation is interrupted by the voltage modulation, resulting in the increase of the growth rate.

On the other hand, SPM local oxidation nanolithography using tapping mode is a useful technique for precise control of the feature size of the oxide wires. Since the SPM tip is excited at its resonance frequency for the tapping mode experiments, it may be possible to neutralize and release the space charge within the oxide [14].

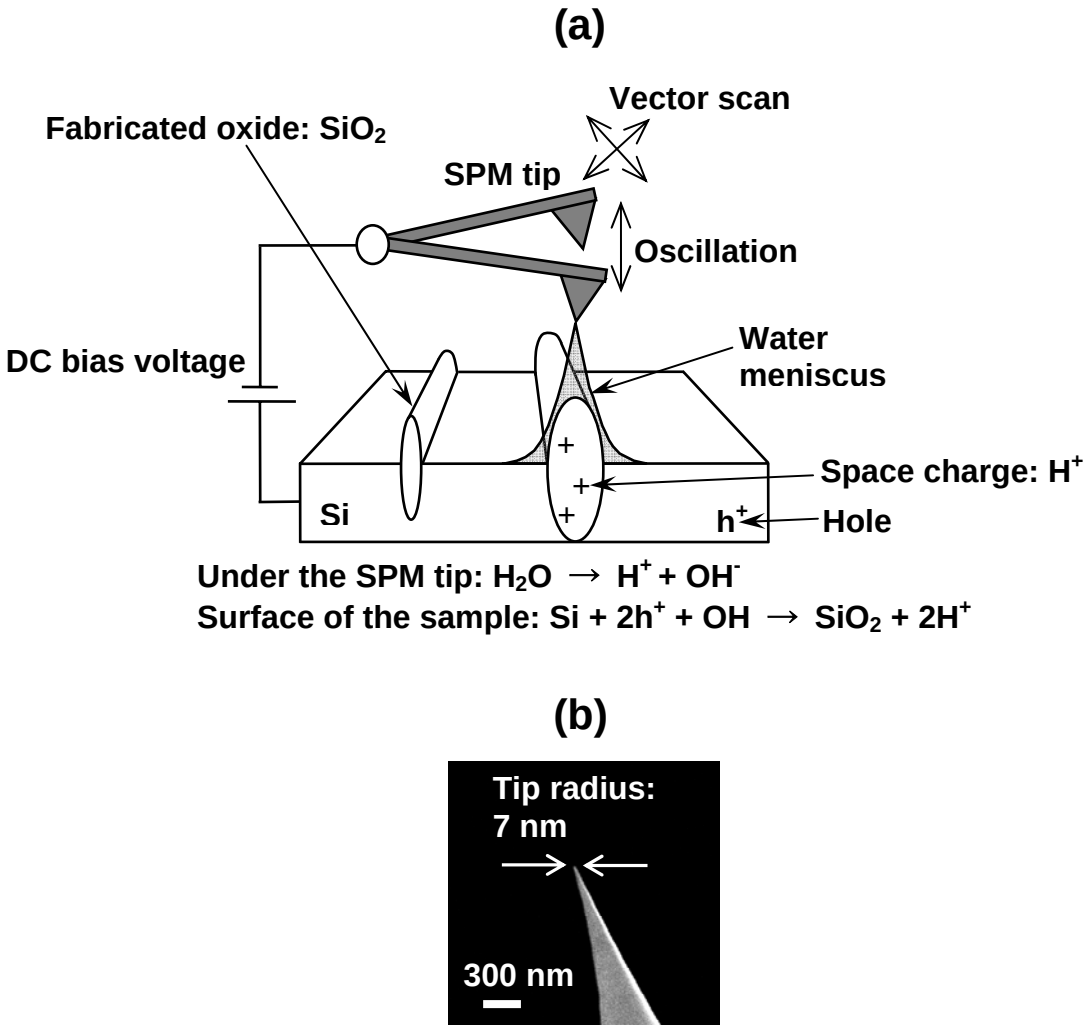


Fig. 3.1. (a)Schematic of local oxidation nanolithography using tapping mode SPM. (b) SEM image of SPM tip for tapping mode operation.

3.3 Nanometer-Scale SPM Local Oxidation Lithography

3.3.1 Effects of Amplitude Modulation of Cantilever on Size of Si Oxide Wires

In tapping mode SPM local oxidation, the cantilever is driven at its characteristic resonance frequency and has a free air amplitude determined by drive amplitude, spring constant and quality factor (Q) of the cantilever's mechanical resonances. Upon approaching the sample, the tip briefly touches, or taps, the surface at the bottom of each swing, resulting in a decrease in oscillation amplitude. As shown Fig. 3.2(a), the feedback loop keeps this decrease at a preset value and a topographic image of the sample surface can be obtained. In the local oxidation process, an initial value of the oscillation amplitude is set to 100 nm or 204 nm with spring constant of 42 N/m or 2 N/m, respectively. Figure 3.2(b) shows the dependence of the oscillation amplitude of the cantilevers on the output voltage of photo detector. The oscillation amplitude is changed by tuning the excitation voltage of the cantilever. It has been reported that the method can improve the force sensitivity of dynamic force microscopy (DFM) including tapping mode in heavily damped environment [15]. Furthermore, quality factor enhancement in magnetic force microscope (MFM) allows the sensitive measurement of the magnetic domain structures in ambient [16]. Since the effects of the dynamic properties of the cantilever are still not clear on the tapping mode SPM local oxidation experiments, the dependence of the feature size of the fabricated oxide on the amplitude of the cantilever is investigated by varying the excitation of the cantilever.

The experiments were performed with an SPM operated in tapping mode (SPA400/SPI4000, SII Nano Technology) in ambient air. The relative humidity was kept at ~30 %. The sample was p-type silicon substrates with a resistivity of ~1 kΩ·cm. Doped n^+-type silicon cantilever was used. As shown in Fig. 3.1(b), the spring constant, the resonance frequency and tip radius of the cantilever were typically 40 N/m, 300 kHz, and 7 nm, respectively.

The amplitude of the cantilever was changed from 45 to 500 nm by tuning the excitation voltage of the cantilever. Size (height and width) dependence of Si oxide wires, formed by changing the amplitude of the cantilever in the tapping mode SPM local oxidation, is shown in Fig. 3.3(a). The width presented here indicates the full width at half maximum (FWHM) of the Si oxide wire. All SPM images in this study were taken in size of 1 x 1 μm^2. In the experiments, the scanning speed was set at 15 nm/s and the applied DC voltage was 20 V. The quality factor of the cantilever was fixed at a natural value of 454. With enhancing the amplitude of the cantilever, the size of the fabricated oxide wires was decreased. Figure 3.3(b) also shows the width and the height of the oxide wires in Fig. 3.3(a). By changing the amplitude of the cantilever from 45 to 500 nm, the feature size of the fabricated oxide was well controlled, ranging from 55 nm to 25 nm in width and 2.2 nm to 0.5 nm in height.

In addition, matrix data of the local oxidation experiments were taken with different DC voltages and amplitudes. The scanning speed and the quality factor were set at 20 nm/s and a natural value of 505, respectively. The DC bias voltage and the amplitude were varied from 20 V to 27.5 V and from 45 to 298 nm, respectively. Figure 3.4(a) shows the SPM images of the matrix data and the size of the oxide wires with different DC voltages is also shown in Fig. 3.4(b). Feature size of the oxide wires is decreased with the increase of the amplitude of the cantilever. Furthermore, as widely known in SPM local oxidation experiments, the size is also well controlled by changing the applied DC voltage.

Figure 3.5 also shows SPM images and cross sections of Si oxide wires as a function of the oscillation amplitude of the cantilever at DC bias voltage of 20 V. The feature size of the fabricated oxide was well controlled and ranged from 31.3 to 18.3 nm in width and from 1.5 to 0.4 nm in height, respectively. The size uniformity of the oxide was evaluated by the standard deviation (STD) of measurements taken from 10 cross sections along the X axis. The STDs of the Si oxide wires were typically 2.1-3.2 nm in width (W_{STD}) and 0.1-0.2 nm in

height (H_{STD}), which were smaller than those (W_{STD} = 9.2 nm, H_{STD} = 0.3 nm) obtained by contact-mode experiments in ref. 17, which is a comparative study of contact-mode and amplitude-modulated tapping-mode experiments.

Figure 3.6(a) shows an SPM image of a Si oxide wire formed by optimizing the oxidation conditions: the applied DC bias voltage of 17.5 V, the scanning speed of 250 nm/s and the oscillation amplitude of 292 nm. Figure 3.6(b) shows the cross-sectional profiles of the Si oxide wire along the X axis. The ten point cross sections were taken at 50 nm intervals along the Y axis. The average width and STD of the width were estimated by the cross sections, which were 9.8 nm and 1.9 nm, respectively. The size fluctuation of the Si oxide wire was further suppressed than that of contact mode experiments (STD of width = 9.2 nm) [17]. Furthermore, the minimum FWHM in the ten cross sections was 8.5 nm.

We consider that the larger amplitude of the cantilever may reduce the spatial dimension of the water meniscus formed between the SPM tip and the sample surface, resulting in the smaller resolution of the fabricated oxide. Additionally, the amplitude enhancement causes to decrease the average intensity of electric field between the tip and the sample. This also contributes to the improved size controllability with smaller resolution of the fabricated oxide. In the tapping mode SPM local oxidation with the modulation of the amplitude of the cantilever, since the SPM tip is excited at its resonance frequency, the space charge accumulated in the oxide is easily neutralized and released by the modulation of the electric field, resulting in the stable oxidation.

Figure 3.7 shows a simple model of tapping mode SPM local oxidation. The lateral dimensions of the water meniscus could be decreased by increasing the tip-surface separation. Amplitude modulation of the cantilever causes the cyclic meniscus formation between the tip and sample surface. Anodic oxidation occurs within the water meniscus, so that the oxidation time τ becomes discrete. In this situation, it seems that the average lateral dimension of the

water meniscus during the oxidation was determined to be below 10 nm, resulting in the formation of Si oxide wire with sub-10 nm dimensions. Moreover, the amplitude enhancement over the maximum length of stretched water meniscus D causes to decrease the average intensity of electric field between the tip and sample. This also contributes to the improvement of size controllability of the oxide with smaller dimensions.

Moreover, standard deviation of the width on the Si oxide wires in Fig. 3.4(a) was typically determined to be around 2.0 nm, so that the variation of the amplitude of the cantilever during the tapping mode SPM local oxidation experiments does not affect the size uniformity of the fabricated oxide wires. These results imply that the SPM local oxidation nanolithography with active control of the cantilever dynamics is a useful technique for producing higher controllability and uniformity of Si oxide wires.

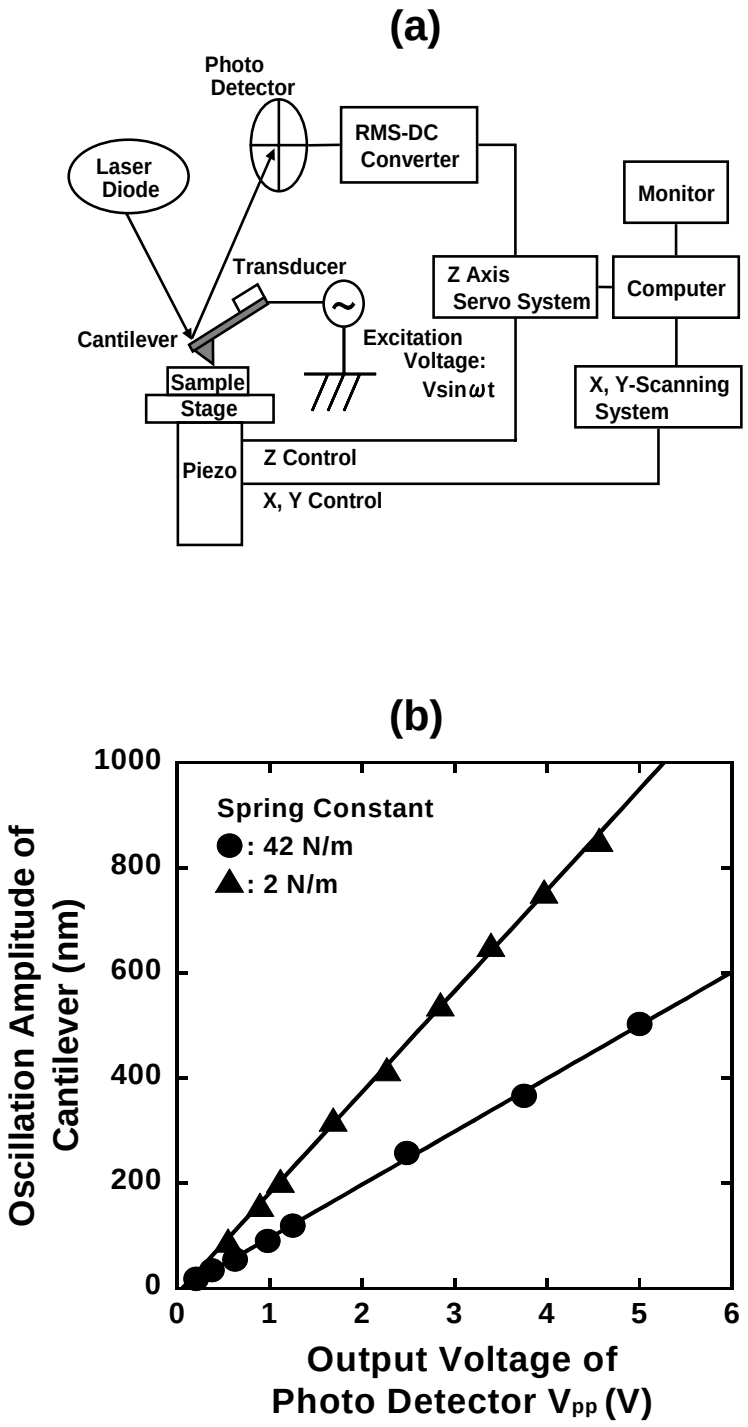


Fig. 3.2 (a) Schematic diagram of a tapping mode operation system. (b) Oscillation amplitude of the cantilever as a function of output voltage (V_{pp}) of photo detector.

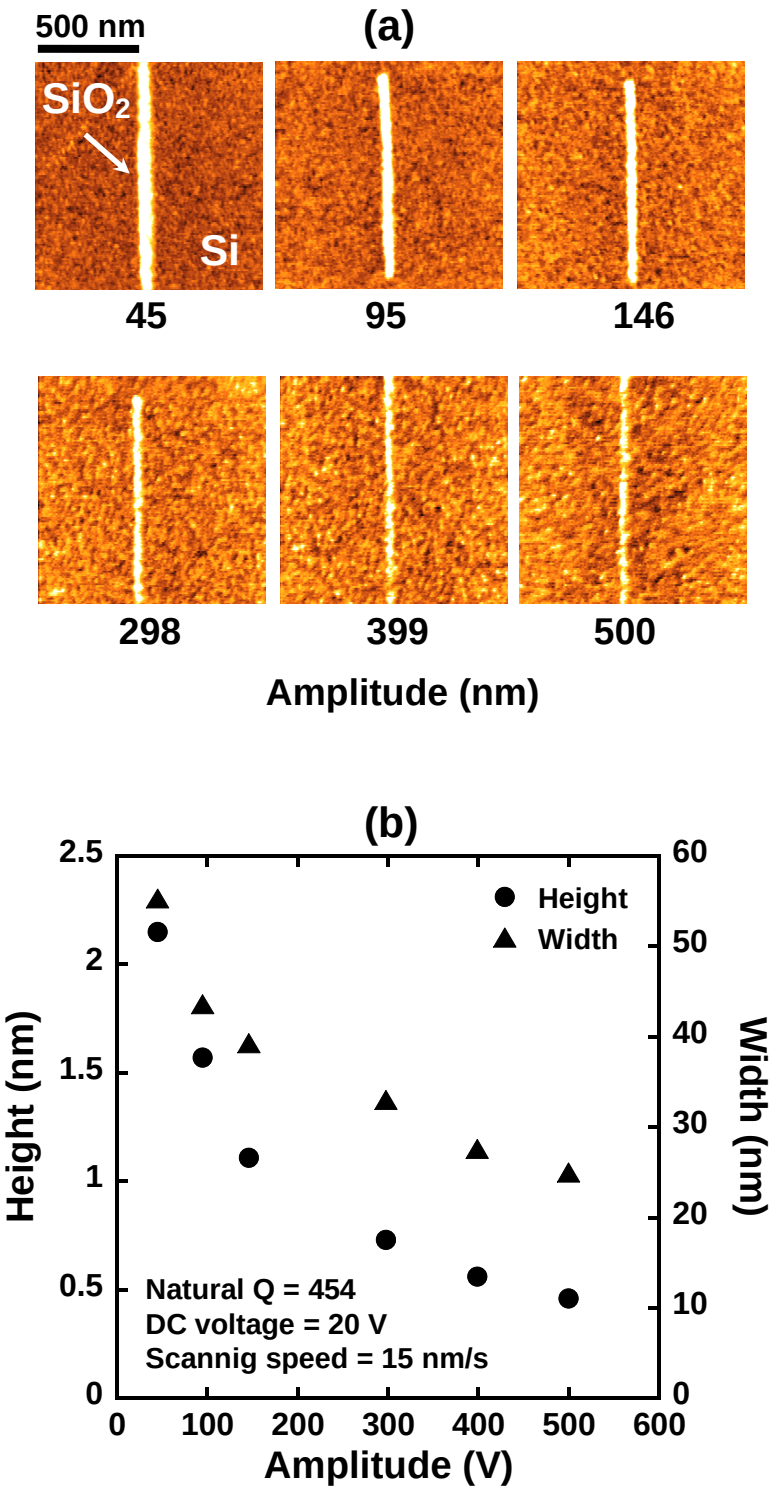


Fig. 3.3 (a) SPM images of tapping mode SPM local oxidation experiments performed for different amplitudes of the cantilever. Quality factor was fixed at a natural value of 454. DC bias voltage applied to the tip and scanning speed of the tip were set at 20 V and 15 nm/s, respectively. (b) Size dependence of Si oxide wires on the amplitude of the cantilever.

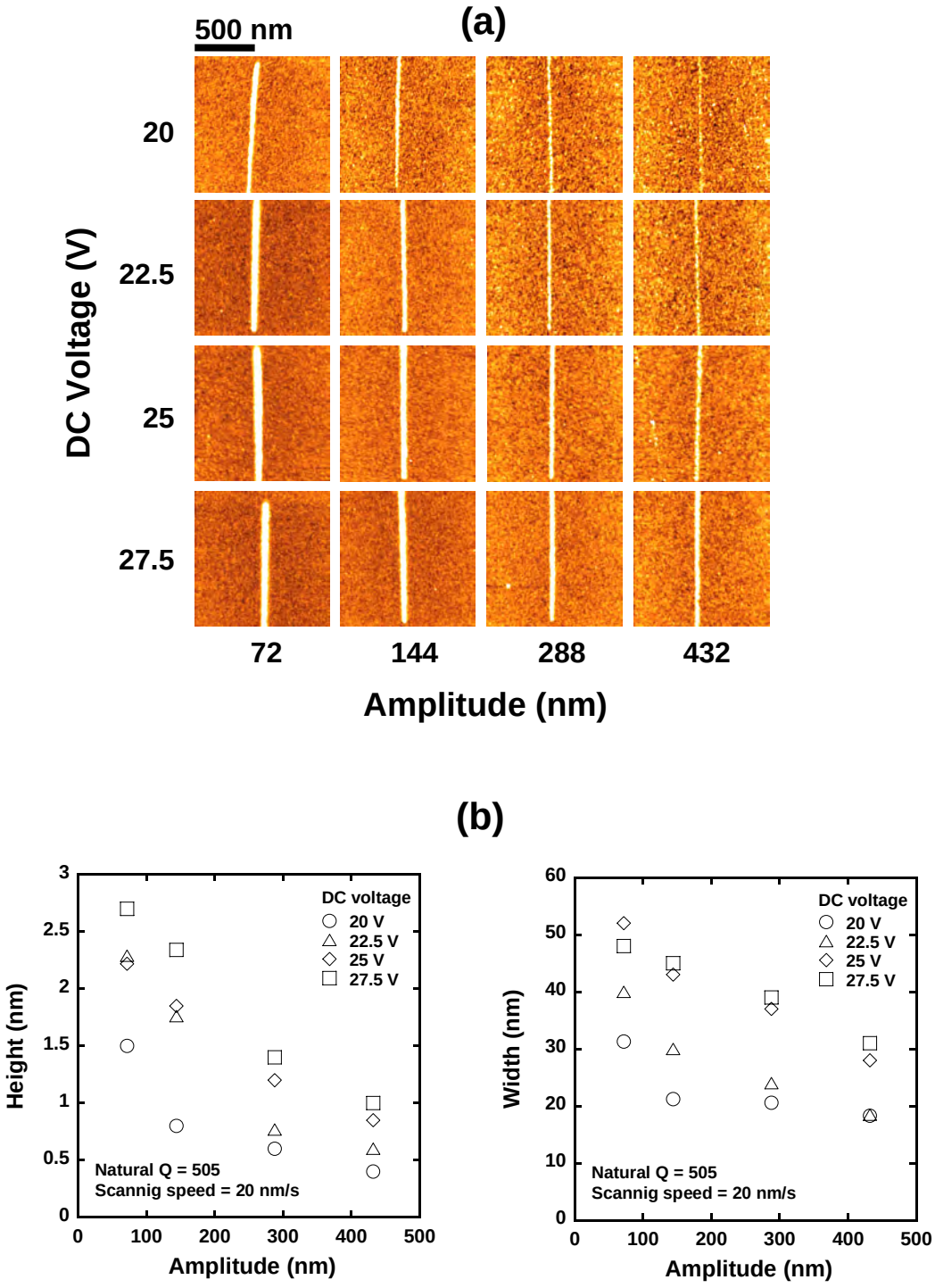


Fig. 3.4 (a) SPM images of tapping mode SPM local oxidation experiments performed for different amplitudes and DC bias voltages. Quality factor and scanning speed of the cantilever were set at 505 and 20 nm/s, respectively. (b) Size dependence of Si oxide wires on the amplitude of the cantilever. Different DC bias voltages were applied to the SPM tip.

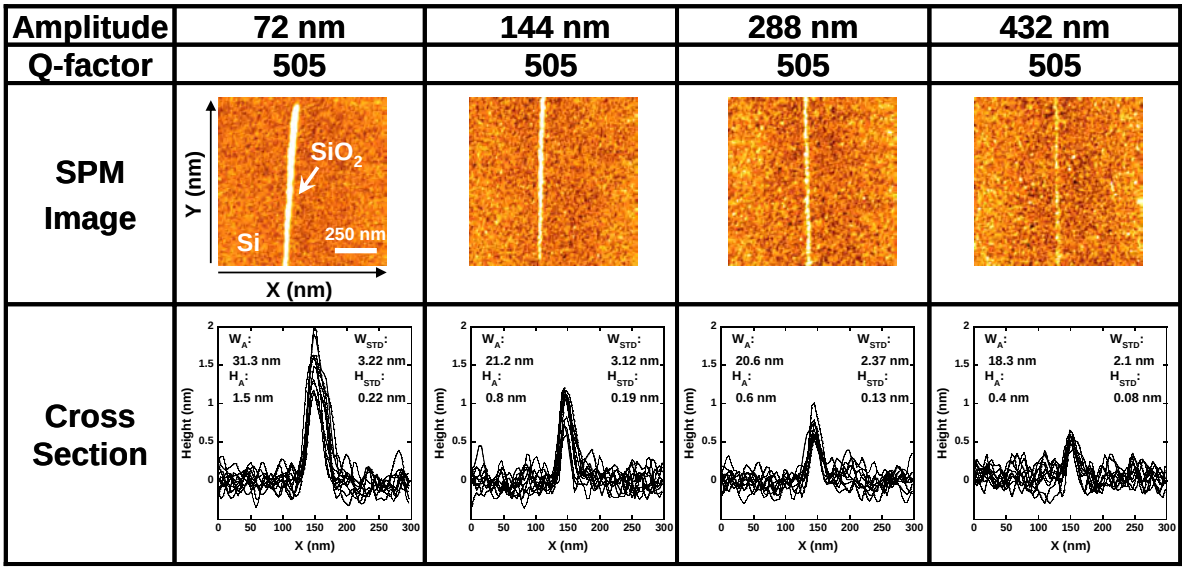


Fig. 3.5 SPM images and cross sections of Si oxide wires formed by amplitude modulation during tapping-mode SPM local oxidation. The oscillation amplitude of the cantilever was varied from 72 to 432 nm. The quality factor was fixed at a natural value of 505. The DC bias voltage applied to the tip and the scanning speed were set at 20 V and 20 nm/s, respectively. W_A and H_A correspond to the average width and average height, taken from 10 cross sections and W_{STD} and H_{STD} represent the STD of the width and height, respectively.

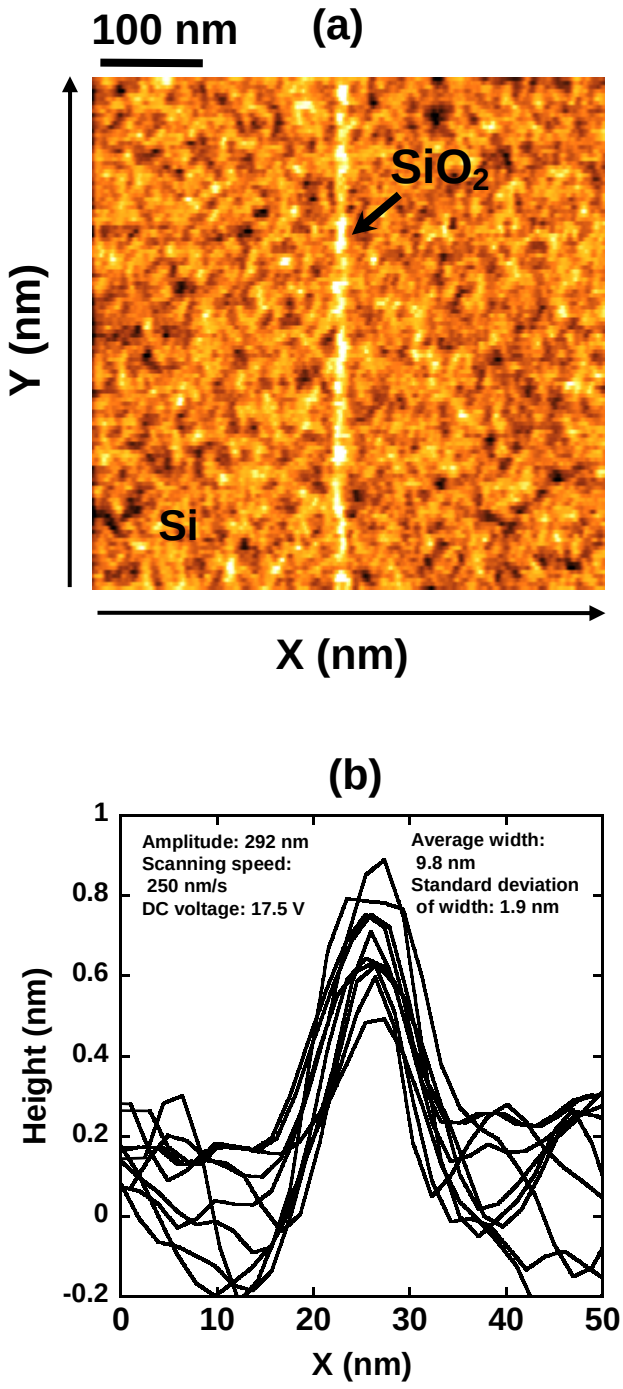
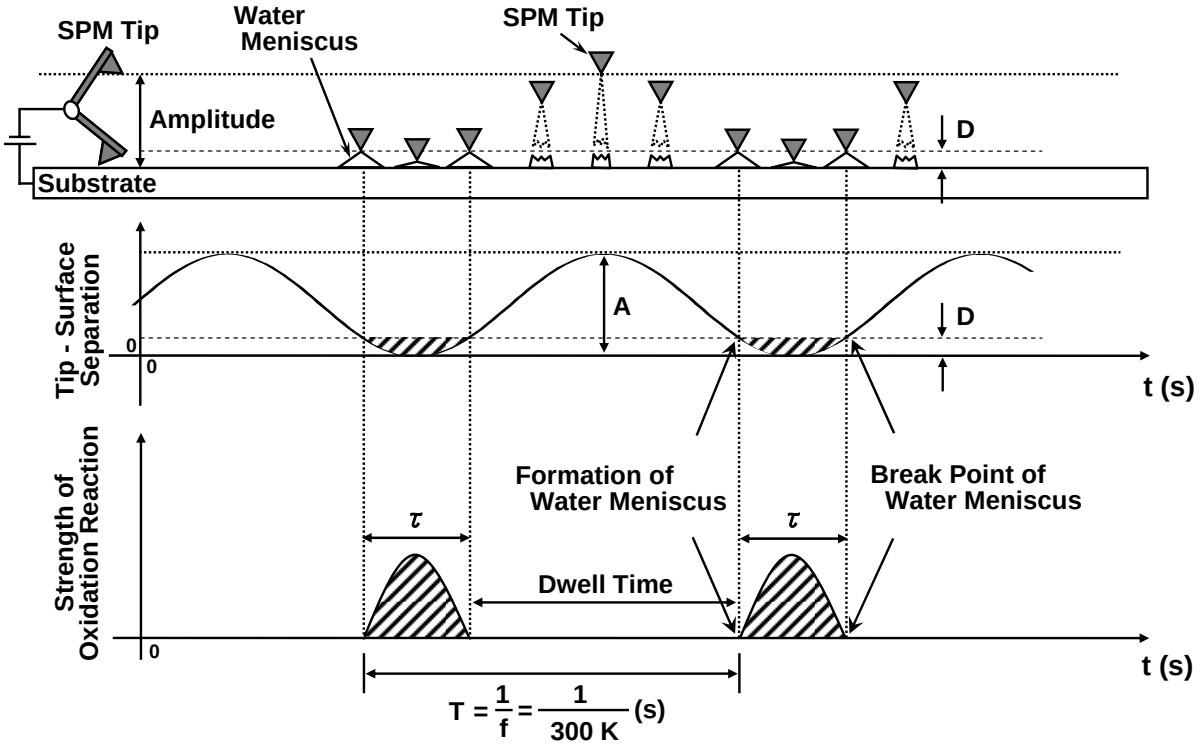


Fig. 3.6 (a) SPM image and (b) cross section of Si oxide wire with sub-10 nm dimensions. Local oxidation was performed by optimizing the control parameters (DC bias voltage = 17.5 V, scanning speed = 250 nm/s, oscillation amplitude = 292 nm).



D: Maximum Length of Stretched Water Meniscus (nm)

A: Amplitude of Cantilever Oscillation (nm)

f: Resonance Frequency of Cantilever (Hz)

R: Oxidation Ratio (%)

$$R = \frac{\tau}{T} \times 100\ (\%)$$

τ : Oxidation Time (s)

T: Period of Cantilever Oscillation (s)

Fig. 3.7 Model of taping mode SPM local oxidation. The oscillation of the cantilever induces the cyclic formation of the water meniscus. The anodic oxidation occurs within the water meniscus and becomes discrete.

3.3.2 Effects of Q-factor Modulation of Cantilever on Size of Si Oxide Wires

The Q-factor of the resonance is defined by $Q = m\omega/\gamma$, where ω is the resonance frequency, m is the effective mass, and γ is the damping factor of the cantilever. The control of the Q-factor was achieved via the implementation of a positive feedback loop. In general, it is difficult to set a stable desired Q-factor in Q-factor-controlled SPM when executing measurements. Therefore, even when a high Q-factor is set, the response is sacrificed and in particular, the stability of the measurement deteriorates. Further, when a low Q-factor is set, there is a problem that high sensitivity in the measurement of the force gradient is difficult [18-20]. Hence, in this study, the Q-factor of the cantilever, which had a natural value of around 500, was varied from 193 to 1665 in order to avoid such difficulties.

In order to perform a direct comparison between amplitude modulation of the cantilever and Q-factor modulation of the cantilever in tapping mode experiments, we have kept unchanged the sample properties, the relative humidity, and other control parameters of Si oxide wires such as bias voltage and scanning speed. The scanning speed and DC voltage were fixed at 20 nm/s and 20 V, respectively, throughout the experiments.

Figure 3.8 shows the Si oxide wires formed with varying the Q-factor. The cantilever initially had oscillation amplitude of 144 nm and a Q-factor of 537. As shown in Fig. 3.8, the feature size of the oxide tends to decrease with increasing the Q-factor. The width and height decreased from 33.7 to 24.9 nm and from 1.2 to 1.0 nm, respectively, with STDs of W_{STD} = 2.0-3.6 nm and H_{STD} = 0.21-0.26 nm. In particular, Figs. 3.5 and 3.8 show that the feature size of the Si oxide wires is more strongly affected by the oscillation amplitude of the cantilever than the Q-factor.

In SPM local oxidation with a controlled Q-factor, since the increase of the Q-factor effectively promotes greater force sensitivity of the cantilever, it is possible to control the motion of the cantilever precisely. Therefore, the fluctuation of the tip-sample distance is

considerably suppressed with the enhancement of the Q-factor. Thus, it seems that the water meniscus between the tip and the sample is more stably formed with a higher Q-factor value, resulting in the precise control of the oxide size. In fact, as shown in Figs. 3.5 and 3.8, the STDs of the size of the fabricated oxide wires are approximately 2-3 nm in width and 0.1-0.2 nm in height and are less dependent on the dynamic properties of the cantilever. It is suggested that the size uniformity of the fabricated oxide wires is unaffected by both the enhancement of the oscillation amplitude and that of the Q-factor. Therefore, tapping-mode SPM local oxidation combining both amplitude modulation and Q-factor control is a useful technique for realizing nanometer-scale Si oxide wires with good size uniformity.

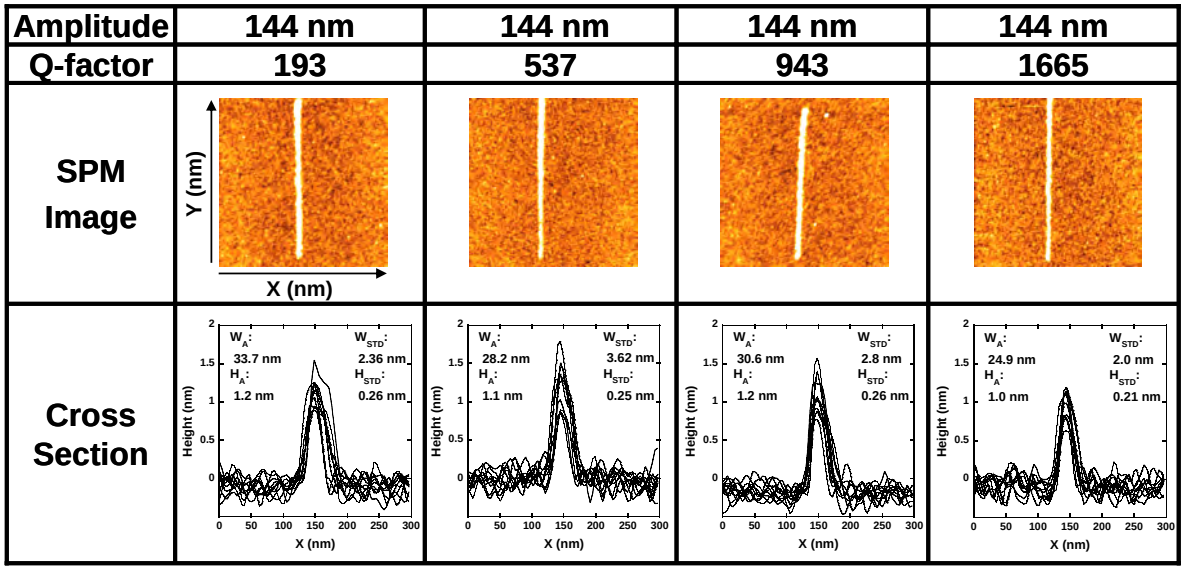


Fig. 3.8 SPM images and cross sections of Si oxide wires formed by Q-factor control during SPM local oxidation. The Q-factor of the cantilever was varied from 193 to 1665. The cantilever initially had an oscillation amplitude of 144 nm and a Q-factor of 537. DC voltage and scanning speed are the same as those in Fig. 3.5.

3.3.3 Analytical Model of Tapping Mode SPM Local Oxidation Based on Oxidation Ratio and Rate Constants

In SPM local oxidation, tapping mode local oxidation nanolithography with active control of the cantilever dynamics is a useful technique for producing higher controllability and uniformity on the nanometer-scale fabrication of Si oxide wires [21]. Furthermore, the direct comparison between contact and tapping mode SPM local oxidation experiments are performed. The standard deviation of the width on the contact and tapping mode experiments was estimated to be 9.2 nm and 2.5 nm, respectively. Thus, the size fluctuation of the Si oxide wires is further suppressed in the tapping mode SPM local oxidation [17]. However, different cantilevers are usually used in comparative studies between contact and tapping mode SPM local oxidation experiments. Ideally, the same cantilever should be used in both local oxidation methods since the size of oxide depends on the tip's size and geometry. In this dissertation, in order to clear the mechanism of SPM local oxidation, we have a comparative study of contact and tapping mode SPM local oxidation experiments with the same SPM tip

Furthermore, for local oxidation kinetics, there has been a quantitative interpretation of experimental kinetic data for SPM oxidation [10]. In contact mode oxidation, an analytical model that explains the behavior of the oxide height with the applied bias voltage and the scanning speed was proposed [22]. It was also reported that the growth rate dependence of Si oxide on the oxidation time is investigated with the rate constant for contact mode oxidation [12].

In order to clear the mechanism of SPM local oxidation, we showed a simple model of tapping mode SPM local oxidation based on the oxidation ratio, which is defined as the oxidation time divided by the period of the cantilever oscillation. In addition, we estimate the oxidation ratio and rate constant for the fabrication of Si oxide wires with 10 nm resolution.

The experiments were performed using an SPM unit (SPA400/SPI4000, SII NanoTechnology) at room temperature. The DC bias voltage was applied to p-type silicon

(100) with a resistivity of 1 kΩ·cm. The silicon native oxide was removed by dipping the sample in HF solution. Ambient air humidity was maintained at 20 %. In order to perform a direct comparison between contact and tapping mode experiments, we have kept unchanged the sample properties, the relative humidity, and other control parameters of Si oxide wires such as bias voltage and scanning speed. Furthermore, the same SPM cantilever was used between both methods. The spring constant and resonance frequency of the Si cantilever were 40 N/m and 300 kHz, respectively. The tip radius is 7 nm. In the experiments, the local oxidation in contact mode operation was performed by applying a contact force as low as possible, which is 78 nN, in order to avoid wear of SPM tip. Because the tip is in contact with the surface, the stiff cantilever is not suitable for the contact mode operation. In contact mode SPM local oxidation, we confirmed that the cantilever is approached to the sample surface during the oxidation by monitoring the deflection of the cantilever. With this method, it is possible to perform contact mode SPM local oxidation with stiff cantilever at lower contact force. In tapping mode SPM local oxidation, the oscillation amplitude of the cantilever was set at 292 nm by tuning the excitation voltage of the cantilever.

Figure 3.9 shows SPM images of (a) contact and (b) tapping mode SPM local oxidation experiments using the same SPM tip at different DC voltages and scanning speeds. The applied bias voltage and scanning speed were varied from 17.5 to 22.5 V and from 250 to 750 nm/s, respectively. All SPM images in this study were of areas of 500 x 500 nm^2. A visual inspection reveals that the Si oxide wires of the tapping mode oxidation are smaller than those of contact mode oxidation. Moreover, the size fluctuation of the Si oxide wires is further suppressed in tapping mode experiments. The cross sections of the Si oxide wires were taken along the X axis in Figs. 3.9(a) and (b). Figures 3.10(a) and (b) show the cross-sectional profiles of the Si oxide wire in contact and tapping mode oxidation with the applied voltage of 22.5 V and the scanning speed of 750 nm/s. Average full width at half maximum (FWHM),

total width (TW) and height were calculated from cross-sectional profiles. To evaluate the size uniformity of the Si oxide wires, the standard deviations (STDs) of FWHM, TW and height were also determined from the cross sections. From Fig. 3.10(b), since the STD of FHWM in tapping mode oxidation is 2.1 nm, the size fluctuation of the oxide is further suppressed than that of contact mode experiments shown in Fig. 3.10(a) (STD of FWHM = 12.2 nm). In Fig. 3.11(a), the FWHM and TW of the Si oxide wires are plotted as a function of scanning speed (DC voltage = 22.5 V). Furthermore, the height and its STD are shown in Fig. 3.11(b). As widely known in SPM local oxidation, the size of the oxide is controlled by changing the scanning speed in both contact and tapping mode oxidation experiments. By changing the scanning speed from 250 nm to 750 nm, the feature size of the oxide in contact mode oxidation is ranged from 62.7 to 54.8 nm in FWHM and from 2.8 to 2.5 nm in height, respectively. Additionally, with increasing the scanning speed, the FWHM and height of the oxide in tapping mode oxidation also decreased from 16.3 nm to 11.0 nm and from 0.6 nm to 0.5 nm, respectively. This result indicates that the smaller resolution of the oxide is realized by tapping mode operation. Furthermore, Fig. 3.11(c) shows the STDs of FWHM and TW of the Si oxide wires. All STDs of FWHM in tapping mode oxidation are below 5 nm, which are smaller than those obtained by contact mode experiments. The relative STDs (RSDs) of FWHM of Si oxide wires fabricated by tapping mode oxidation are approximately 20 %. A similar behavior is also seen in tapping mode Si oxide wires with RSDs higher than 10 % [21]. Since local oxidation experiments are performed under the same conditions including the cantilever, the feature size of the Si oxide wires is strongly affected by SPM modes of operation.

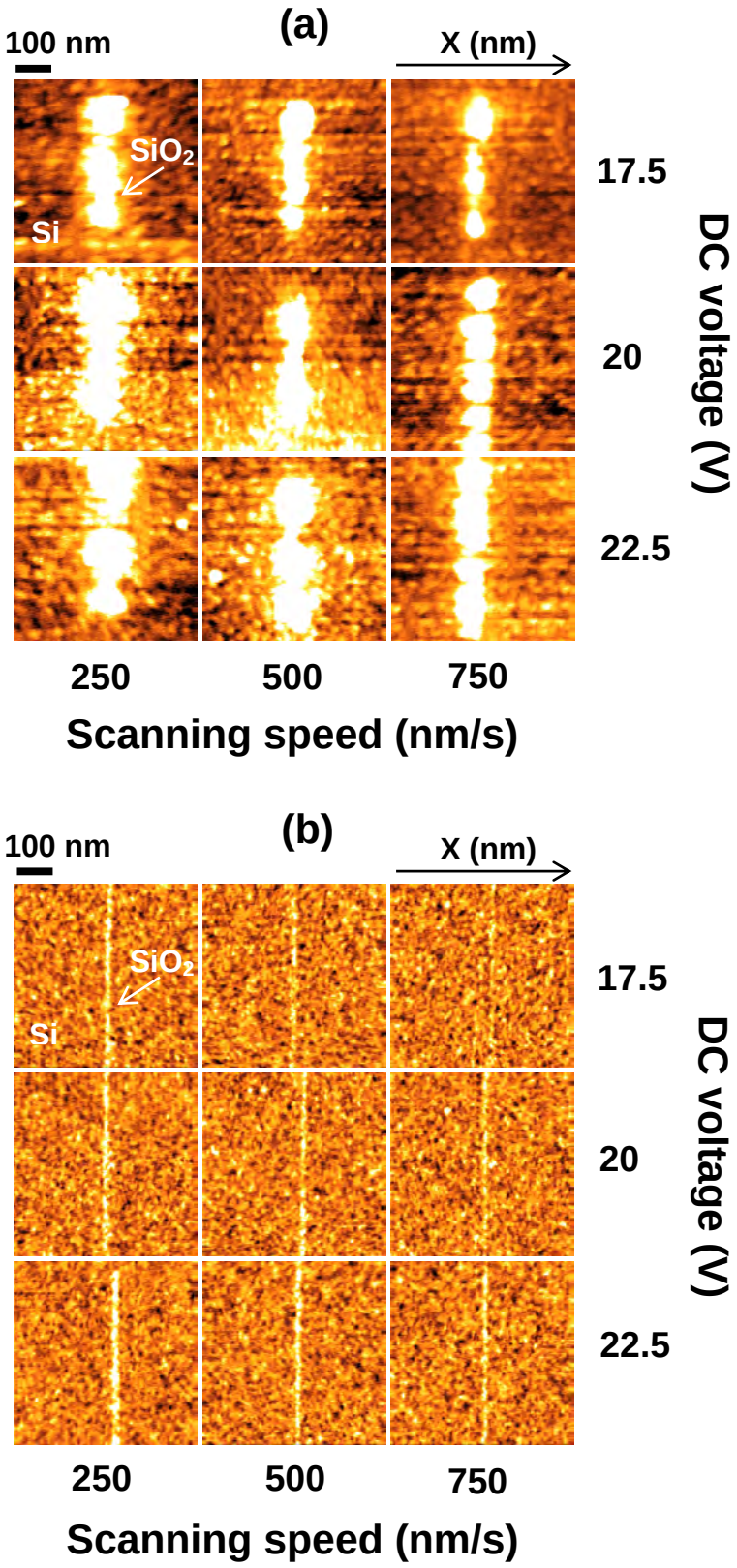


Fig. 3.9 SPM images of (a) contact mode and (b) tapping mode SPM local oxidation experiments with different DC bias voltages and scanning speeds. The same SPM tip is used between contact and tapping mode local oxidation.

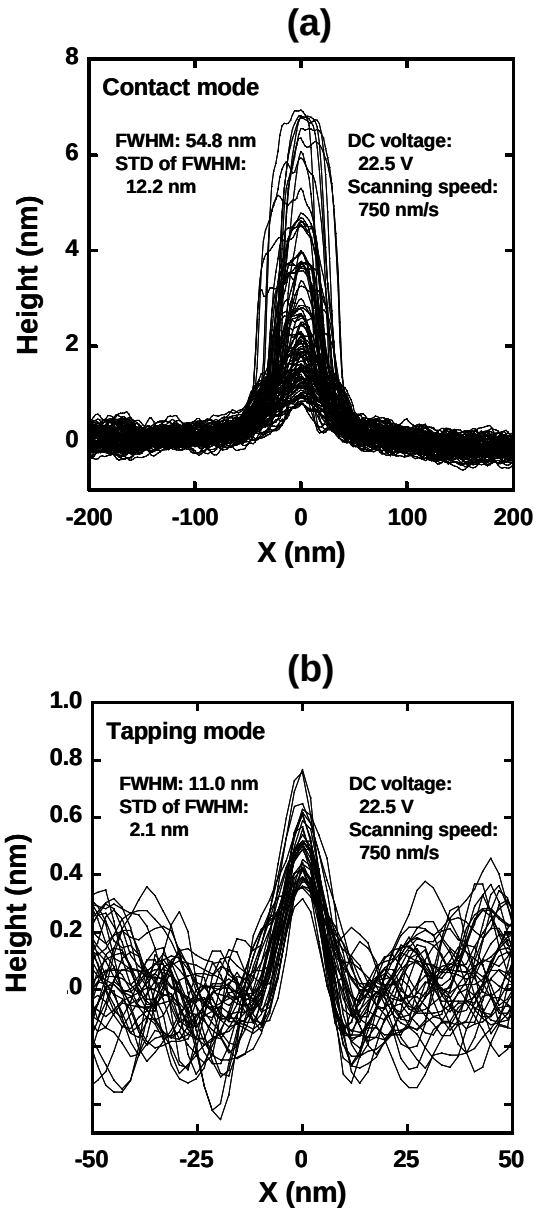


Fig. 3.10 Cross sections of Si oxide wires fabricated by (a) contact mode and (b) tapping mode SPM local oxidation experiments using the same SPM tip (DC bias voltage = 22.5 V, scanning speed = 750 nm/s). The cross sections were taken along the X axis.

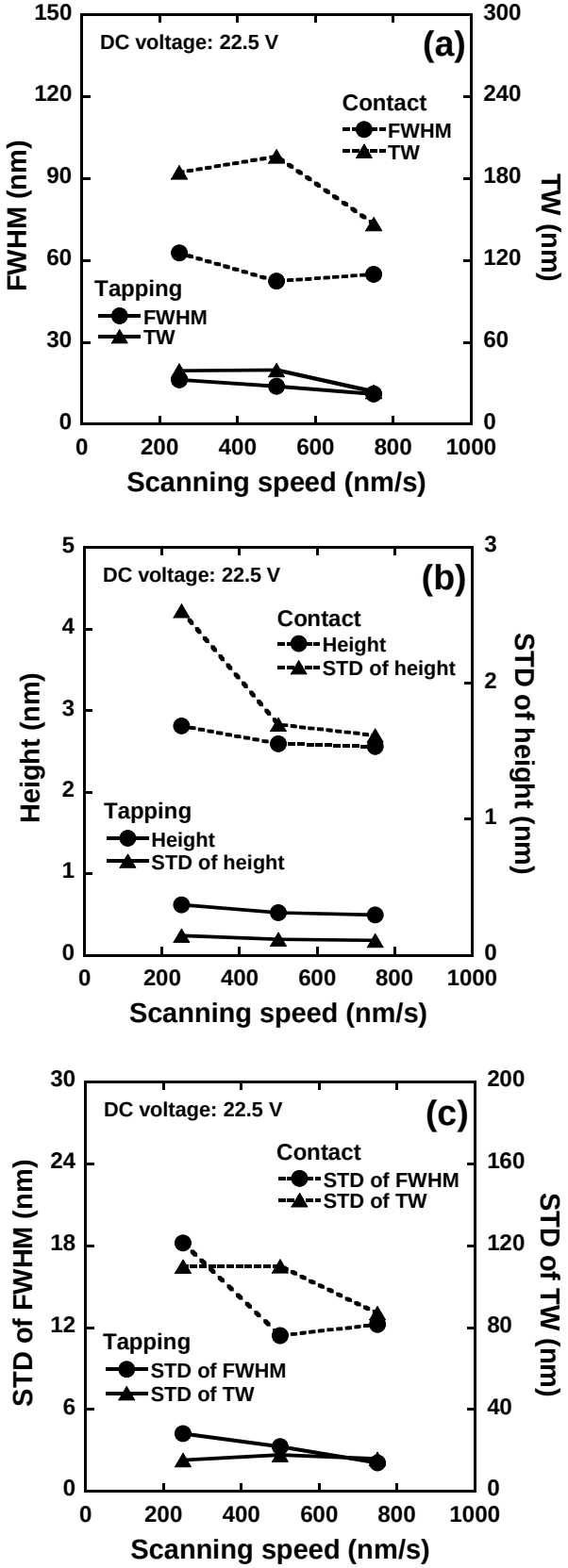


Fig. 3.11 Dependence of (a) FWHM and TW (b) height and its standard deviation (c) standard deviations of FWHM and TW of Si oxide wires on scanning speed of the cantilever.

In order to understand the advantages of tapping mode operation on both controllability and uniformity of the oxide formation, the oxidation reaction induced by the tapping mode operation is considered with a model based on the oxidation ratio and the rate constant. First, we propose an analytical model of tapping mode SPM local oxidation with respect to the oxidation ratio R. R is defined as

$$R\,(\%) = \frac{\tau}{T} \times 100, \tag{3.1}$$

where τ is the oxidation time and T is the period of cantilever oscillation. The motion of cantilever with a respect to time t is expressed as

$$y = \frac{A}{2}\sin\omega t + \frac{A}{2}\left(-\frac{\pi}{2\omega} \le t \le \frac{\pi}{2\omega}\right) \tag{3.2}$$

$$y = D \tag{3.3}$$

where, *A* is the oscillation amplitude of the cantilever. Here, the maximum length of stretched water meniscus is defined as the symbol of D. From the two equations of (3.2) and (3.3), the time of formation and break point of water meniscus is described as t_1 and t_2, respectively,

$$t_1 = \frac{1}{2}T - \frac{1}{\omega}\sin^{-1}\left(\frac{2D - A}{A}\right), \tag{3.4}$$

$$t_2 = \frac{1}{\omega}\sin^{-1}\left(\frac{2D - A}{A}\right) + T, \tag{3.5}$$

Then, the oxidation time τ is expressed as follows,

$$\tau = t_2 - t_1 = \frac{T}{\pi}\sin^{-1}\left(\frac{2D - A}{A}\right) + \frac{1}{2}T. \tag{3.6}$$

Finally the analytical model of tapping mode SPM local oxidation with respect to the oxidation ratio R is described as

$$R\,(\%) = \frac{\tau}{T} = \left(\frac{1}{\pi}\sin^{-1}\left(\frac{2D - A}{A}\right) + 0.5\right) \times 100, \tag{3.7}$$

where τ is the oxidation time, T is the period of cantilever oscillation, A is the oscillation amplitude of the cantilever, and D is the maximum length of stretched water meniscus. This model is also shown in Fig. 3.7. Figure 3.12 shows the oxidation ratio and the FWHM of Si oxide wires as function of the oscillation amplitude of the cantilever. Solid circles represent the experimental data with the scanning speed of 20 nm/s. With enhancing the oscillation amplitude of the cantilever from 23 to 432 nm, the FWHM of the oxide is clearly decreased from 67 to 20 nm. This analytical model provides a good fit to the experimental data when the D ranges from 10 to 25 nm. It is considered that contact mode oxidation has no dwell time and shows the 100 % oxidation ratio. In this fitting model, the 100 % oxidation ratio corresponds to the 150 nm oxide width, which is consistent with the maximum width of the Si oxide formed by the conventional contact mode oxidation [9]. Furthermore, the experimental data (V = 22.5 V) of tapping mode oxidation in Fig. 3.9(b) are also plotted in Fig. 3.12. Open triangle, square, and circle represent the FWHM of the oxide when the scanning speed is set at 250 nm/s, 500 nm/s, and 750 nm/s, respectively. As shown in this figure, maximum length of the water meniscus is deduced to be approximately 10 nm in our fitting procedure. Hence, it is suggested that the oxidation ratio becomes 10-16 % in order to realize the stable local oxidation with sub-10 nm resolution [23]. Since the anodic oxidation occurs within the water meniscus, the average lateral dimension of the water meniscus during the tapping mode oxidation is around 10 nm in this situation. Additionally, the average intensity of electric field strength is reduced due to tapping mode operation, so that this also contributes to the smaller resolution of the oxide [24].

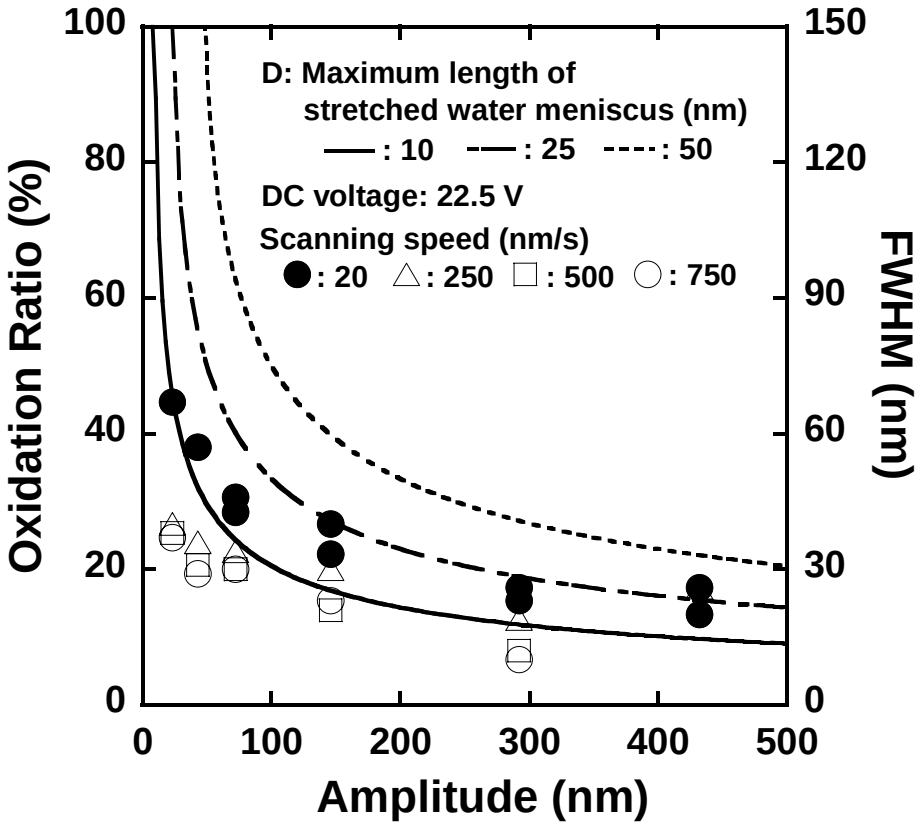


Fig. 3.12 Oxidation ratio and FWHM as function of oscillation amplitude. DC bias voltage is set at 22.5 V. Solid circles represent the experimental data with the scanning speed of 20 nm/s as the oscillation amplitude of cantilever is varied from 23 nm to 432 nm. Open triangle, square, and circle represent the FWHM of the oxide as the scanning speed is set at 250 nm/s, 500 nm/s, and 750 nm/s, respectively.

Here, we consider the rate constant k s^{-1} for SPM local oxidation reaction. In general, the rate constant is determined by measuring the concentration of the species for the reaction [25]. The direct pathway for reaction of oxyanions with silicon at the Si/SiO_2 interface is given by ($[OH^-] \rightarrow [SiO_2]$) and an indirect reaction pathway, mediated by trapped charge defects at the interface, is given by ($[OH^-] \rightarrow [H_3O^+\text{-}OH]$) followed by ($[H_3O^+\text{-}OH] \rightarrow [SiO_2]$) . Then, the rate equation at two path ways is expressed as follows,

$$\frac{d[OH^-]}{dt} = -k_1[OH^-] - k_4[OH^-] = -(k_1 + k_4)[OH^-], \tag{3.8}$$

$$\frac{d[H_3O^+ - OH]}{dt} = k_1[OH^-] - k_3[H_3O^+ - OH], \tag{3.9}$$

$$\frac{d[SiO_2]}{dt} = k_3[H_3O^+ - OH] + k_4[OH^-], \tag{3.10}$$

where, k_1, k_3, and k_4 are the rate constants at two reaction pass ways. In accordance with the model described by Dagata et al., the height of the Si oxide is proportional to the concentration of SiO_2 and is expressed in the following formula:

$$h(t) \propto [SiO_2(t)] = [A_0]\left(1 - e^{-k_3 t} + \frac{k_4 - k_3}{k_3 - (k_1 + k_4)}\left(e^{-(k_1+k_4)t} - e^{-k_3 t}\right)\right), \tag{3.11}$$

where $h(t)$ is the oxide height, $[SiO_2(t)]$ is the evolution of the SiO_2 concentration, t is the oxidation duration, $[A_0]$ is the initial concentration of oxyanions, k_4 is the rate constant for the direct oxidation process, and k_1 and k_3 are the rate constants for indirect reaction mediated by trapped charge defects at the growing interface. In this model, Dagata also shows that the empirical power low, $[SiO_2(t^{\gamma})]$, provides a good fit to the experimental data, where γ is 0.4 for contact mode SPM local oxidation. We investigate the rate constant between contact and tapping mode SPM local oxidation experiments. Oxidation was performed under the applied bias voltage of 22.5 V in contact and tapping mode experiments. Figure 3.13 shows the height of Si oxide dots as a function of oxidation time. As the rate constants are assumed to be k_1 =

4.3×10^{0} s^{-1}, $k_3 = 3.5\times10^{-3}$ s^{-1}, and $k_4 = 2.5\times10^{-1}$ s^{-1}, the model with $\gamma = 0.4$ provides a good fit to the experimental data of contact mode oxidation. On the other hand, in tapping mode experiments, the experimental data are clearly fitted by the model assuming that the rate constants are $k_1 = 1.3\times10^{1}$ s^{-1}, $k_3 = 4.2\times10^{-2}$ s^{-1}, and $k_4 = 1.3\times10^{0}$ s^{-1}. This result indicates that all the rate constants in tapping mode oxidation are larger than those of contact mode oxidation, suggesting that the anodic oxidation is enhanced in tapping mode operation. In contact mode oxidation, it is considered that the space charge is accumulated in the oxide and prevents further growth of the oxide [13]. The cantilever vibrates at the resonance frequency in tapping mode operation, so that the electric field strength between SPM tip and sample surface is strongly modulated in tapping mode oxidation with DC bias voltage. In other words, the electric field depends on the distance between the SPM tip and sample surface and is stronger when the tip is closer to the surface. It is known that the effective diffusivity of H^+ in p-type silicon increases with the increase of electric field [26]. If the similar electric field effect occurs during the Si oxide formation in tapping mode operation, the diffusivity of space charges in the oxide may be enhanced with the oscillating motion of the cantilever, as shown in Fig. 3.14(a) and (b). Therefore, it seems that space charges involved within the Si oxide are easily neutralized and released by the electric field effect. This effect could play an important role for stable SPM oxidation. Finally, the height of the Si oxide as a function of oxidation time in contact and tapping mode is shown in Fig. 3.14(c). From the figure, anodic oxidation is clearly enhanced in tapping mode operation.

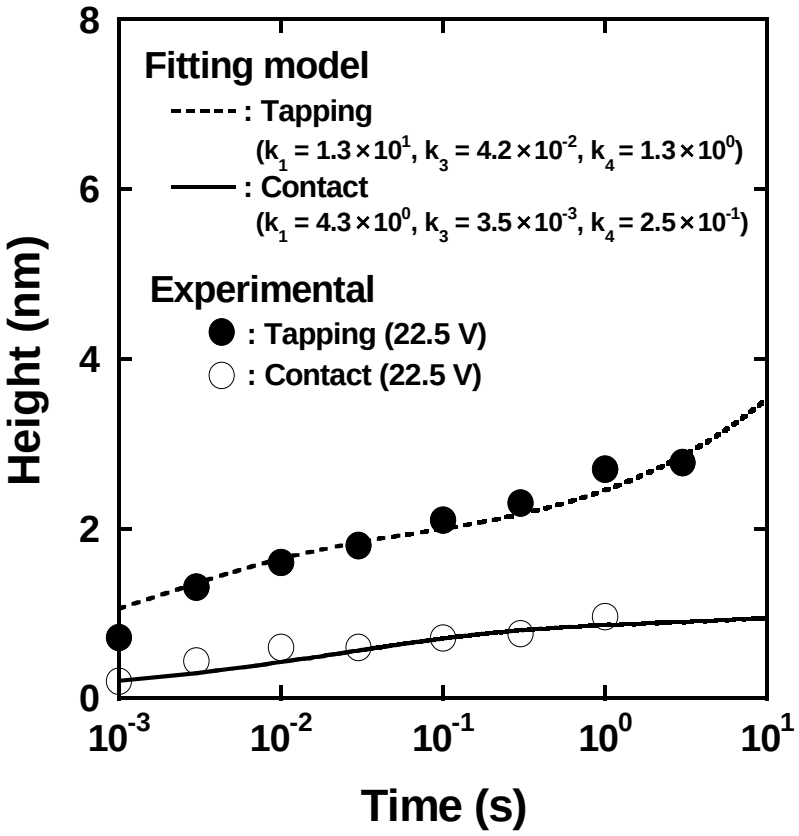


Fig. 3.13 Height of Si oxide formed by contact and tapping mode SPM local oxidation as a function of oxidation time. Solid and open circles show the experimental data of tapping and contact mode SPM local oxidation, respectively.

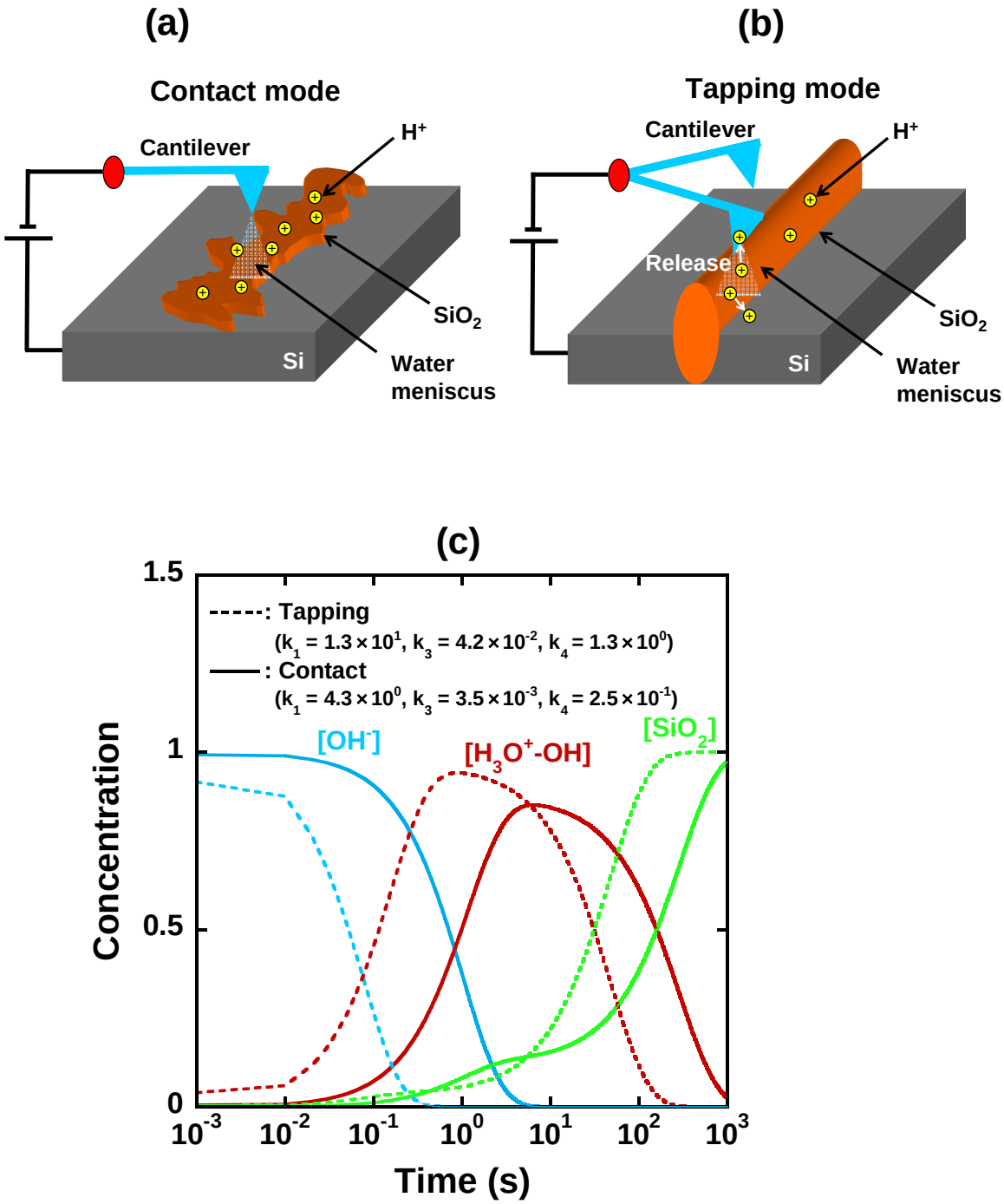


Fig. 3.14 SPM local oxidation in (a) contact and (b) tapping mode operation. (c) Height of Si oxide formed by contact and tapping mode SPM local oxidation as a function of oxidation time.

3.4 Micrometer-Scale SPM Local Oxidation Lithography

The advantages of SPM local oxidation are its operation in ambient air, the simple production of nanometer-scale structures, and fabrication without masks or lift-off processes. On the other hand, in terms of writing speed, conventional SPM local oxidation has a low throughput (defined as the oxide area divided by the writing time) of 0.027 $\mu m^2/s$ [10]. Thus, in view of device applications, it is considered that conventional SPM-based nanolithography is not suitable in terms of the fabrication throughput because nanometer-scale devices such as SETs are composed of submicrometer-scale current confinement structures and micrometer-scale device separation/isolation regions. Here we present a new concept for the fabrication of nanometer-scale devices based on SPMs having different sizes of SPM tips, which have been designed to increase the throughput. Our method involves two SPM tips, one having a robust blunt tip, a “micrometer tip”, and the other having a sharp tip, a “nanometer tip”. By means of an automatic SPM tip changer, the concept of which is introduced in ref. 27, the tip can be changed to switch between large-scale SPM local oxidation with the micrometer tip, and high-resolution SPM local oxidation with the nanometer tip. Hence, the delicate nanometer tip is used only when nanometer-scale tunnel junctions are required. A large-area, oxidized structure is used for lateral current confinement and device separation/isolation. In order to fabricate these micrometer areas with high throughput, a novel local-oxidation technique is developed in this study.

In SPM local oxidation, the application of a voltage between an SPM tip and the sample surface induces the formation of a water meniscus. The size of the water meniscus is important in determining the size of the oxide area formed, since the anodic oxidation reaction is confined within the meniscus diameter [6]. The lateral dimension of the locally formed oxide depends on several factors such as applied voltage [24], scanning speed [22], relative

humidity [28], and tip radius [29]. Therefore, the tip radius is considered to be an important parameter for performing micrometer-scale local oxidation.

In order to upscale the oxide area, it has been reported that a method of patterning millimeter-square areas by parallel local oxidation using a stamp brought into contact with a Si oxide surface should be used [30]. This technique has allowed the patterning of a 5 × 6 mm^2 region with submicrometer motif of 50 ms. However, local oxidation by parallel writing using stamps has some shortcomings. First, it is difficult to pattern a wide variety of feature sizes simultaneously. Second, there is a disadvantage of the overlay accuracy.

In this study, we propose and demonstrate a method of performing micrometer-scale SPM local oxidation using a cantilever with a large tip radius under contact-mode SPM operation. SPM local-oxidation lithography has the advantage of being able to fabricate a desired structure at an arbitrary position on a surface. We show that lithography by SPM is a novel technique for the realization of high fabrication throughput for micrometer-scale systems.

The relative humidity was kept around 40 - 45 %. The sample was p-type silicon (100) with a resistivity of 1 kΩ·cm. The top view of an SPM tip used in this study and a schematic of micrometer-scale SPM local oxidation are shown in Figs. 3.15(a) and (b), respectively. In order to produce large-scale oxidation, a silicon cantilever with a contact area of 2.5 × 1.9 μm^2, which is about 12,000 times larger than that of a conventional SPM tip, was prepared. The spring constant was typically 15 N/m. Under the scan direction shown in Fig. 3.15(a), the contact length between the tip and the water meniscus is defined as the larger dimension of the contact area and is typically 2.5 μm. Furthermore, other experiments were also realized using the cantilever with a contact length of 2.2 μm, in order to investigate the size dependence of the oxide area on the contact length of the cantilever. The size evaluation of the oxidized area was performed by SPM and scanning electron microscopy (SEM).

Figure 3.16 shows images of micrometer-scale SPM local-oxidation experiments at different DC voltages and scanning speeds. The contact length of the cantilever was 2.5 μm. The applied bias voltage and scanning speed were varied from 3 to 7 V and from 0.5 to 50 μm/s, respectively. As shown in Fig. 3.16, the threshold voltage for Si oxide formation is obtained to be approximately 3 V, which is comparable to that of conventional contact-mode SPM local oxidation [11, 31]. For contact-mode SPM oxidation with a 2.5 μm tip, an applied voltage above 3 V and a scanning speed below 50 μm/s are needed to form the oxide with good size uniformity. Moreover, the width of the oxide formed does not depend on the bias voltage provided it is above the threshold, but the height is weakly influenced by the scanning speed. It seems that the height uniformity is improved by increasing the applied voltage even at a high scanning speed. As expected, the width of the Si oxide formed is determined by the contact area of the SPM tip because the anodic oxidation occurs within the water meniscus beneath the tip. In other words, the lateral dimension of the water meniscus corresponds to the contact area of the tip.

The width dependences of the Si oxide region on the DC voltage and scanning speed of the cantilever are also shown in Figs. 3.17(a) and 3(b), respectively. Two cantilevers with different contact lengths of 2.5 and 2.2 μm were used in the experiments. As shown in Figs. 3.17(a) and 3(b), an oxide region with 2.5 μm width is produced by the cantilever with 2.5 μm contact length, and a region of 2.2 μm width is produced for the 2.2 μm contact length. This clearly suggests that the width of the Si oxide region is not significantly affected by the applied voltage provided it is above the threshold nor the scanning speed but is completely determined by the contact length of the cantilever. With respect to the Si oxide fabricated with the 2.5 μm tip, Figures 3.18(a) and (b) show the height dependences of the oxide region on the bias voltage and scanning speed, respectively. The height grows with increasing the bias voltage and decreasing the scanning speed. This tendency is similar to the results reported for

conventional contact-mode SPM local oxidation with a nanometer tip [31, 32]. Therefore, it is believed that the oxidation mechanism is essentially the same for micrometer and nanometer tips. Since the size variation of the water meniscus during SPM local oxidation under a typical bias voltage is considered to be in the range of a few tens of nm [6], the size of the micrometer-scale water meniscus is not significantly affected by oxidation parameters such as applied bias voltage above the threshold or the scanning speed. Therefore, the lateral dimension of the water meniscus is well defined by the contact area of the cantilever, resulting in the fabrication of the Si oxide region with the same size as the meniscus.

Throughput, which is defined as the oxide area divided by the writing time, as a function of the scanning speed is shown in Fig. 3.19. Throughput increases almost linearly with the scanning speed. This is due to the fact that the width of the Si oxide region is dominantly controlled by the contact length of the cantilever and does not depend on the applied voltage or the scanning speed. In the experiments, when the local oxidation conditions were 50 μm/s and 7 V, the throughput reached 125 $\mu m^2/s$, which is 10,000 times larger than that of conventional SPM local oxidation. Since the curvature radius of the tip is around 10-20 nm in conventional contact-mode SPM local oxidation, it takes considerable time to realize a micrometer-scale Si oxide region. The cantilever with a larger tip radius of over 2 μm markedly increases the spatial dimension of the water meniscus and produces a larger reactive area, resulting in a larger area of the fabricated oxide. These results imply that the realization of micrometer-scale SPM local oxidation is possible with a micrometer-scale SPM tip.

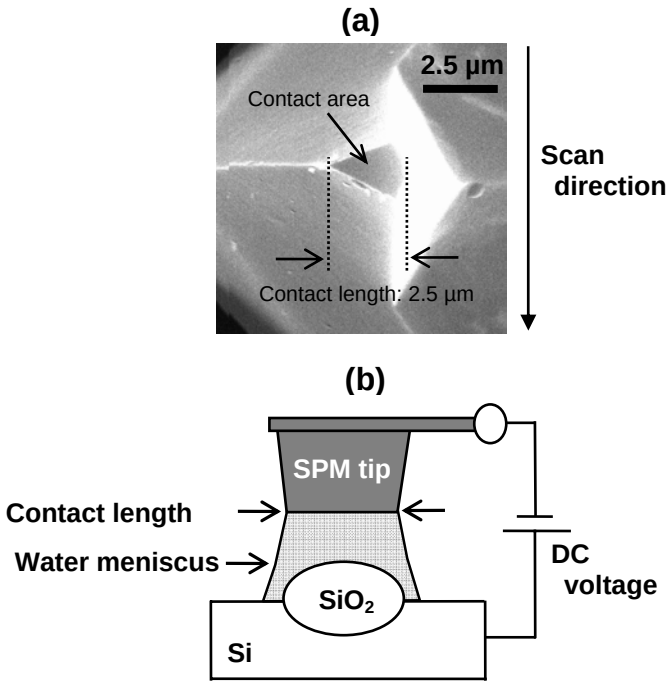


Fig. 3.15 (a) SEM image of an SPM tip (top view) used for micrometer-scale SPM local oxidation. The effective contact area of the cantilever with the sample surface is 2.5 × 1.9 μm^2. (b) Schematic of micrometer-scale SPM local oxidation.

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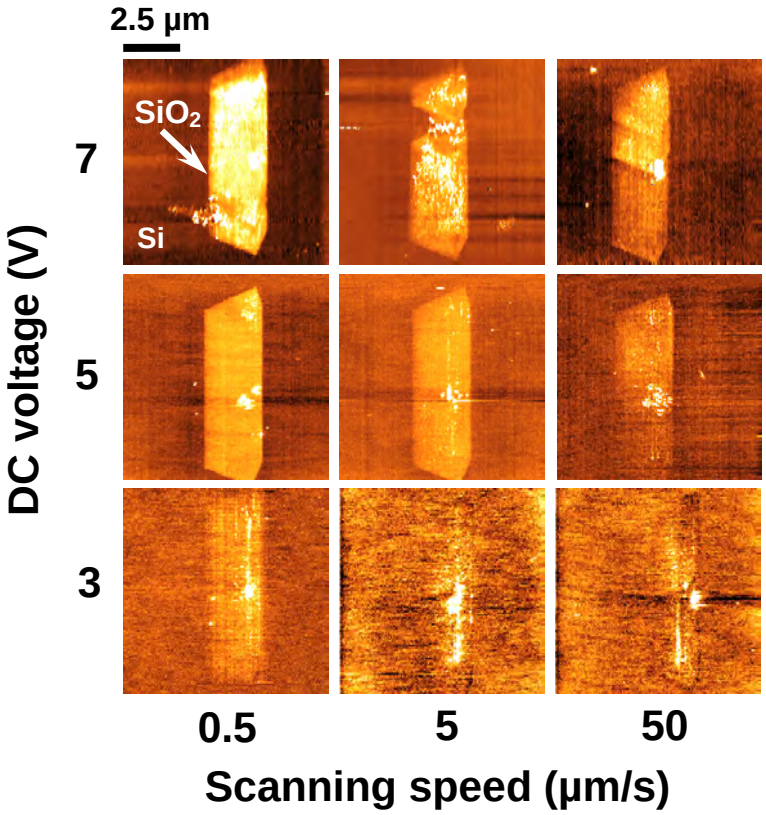


Fig. 3.16 Images of micrometer-scale SPM local-oxidation experiments performed for different DC bias voltages and scanning speeds. The contact length of the cantilever is 2.5 µm.

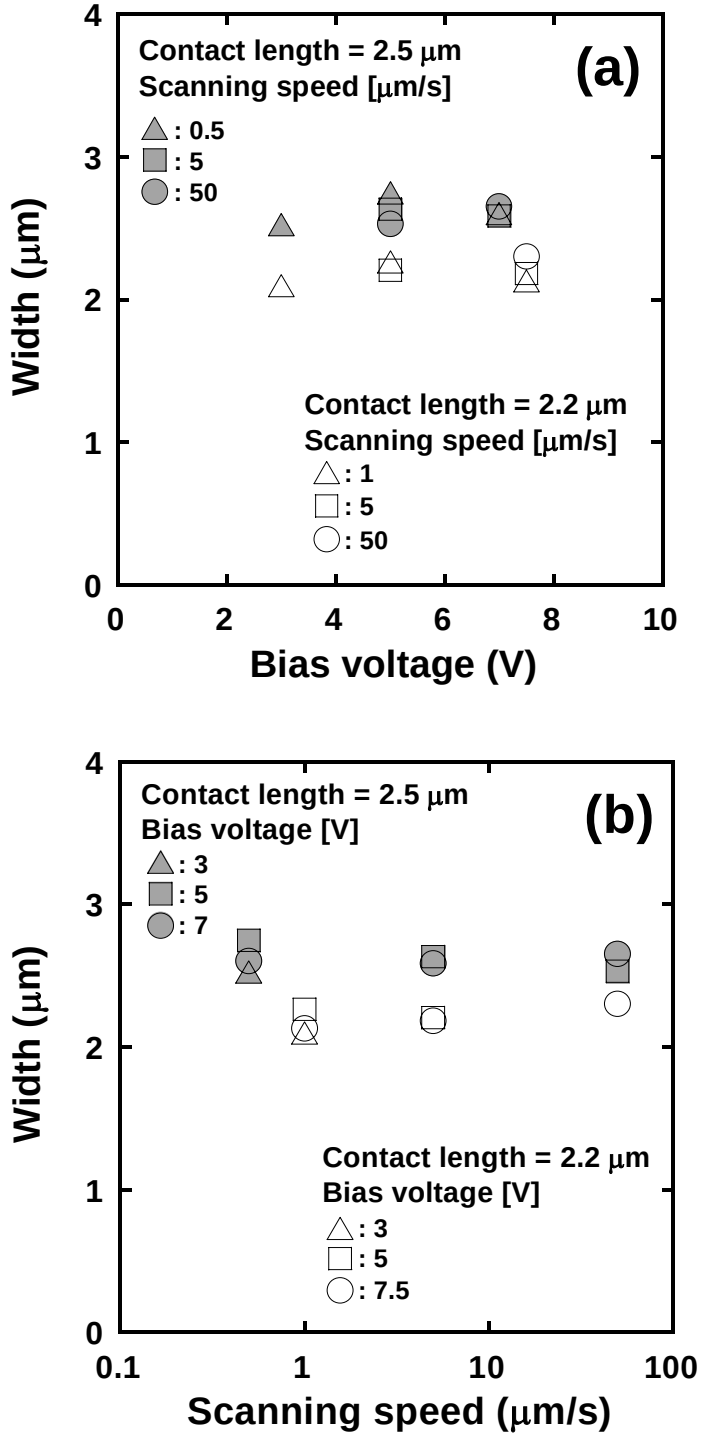


Fig. 3.17 Width dependences of the Si oxide region on (a) DC bias voltage and (b) scanning speed. Gray and white symbols correspond to cantilevers with contact lengths of 2.5 and 2.2 μm, respectively.

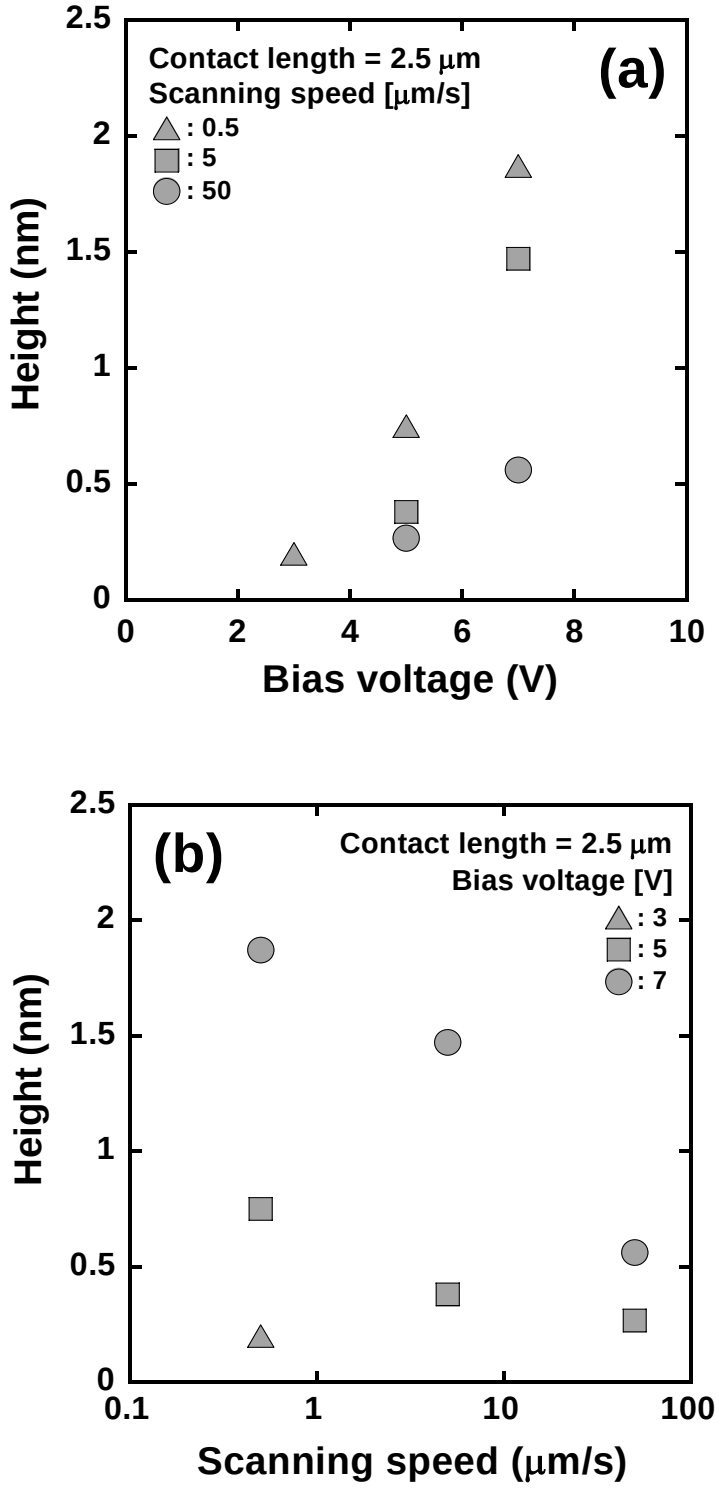


Fig. 3.18 Height dependences of the Si oxide region on (a) DC bias voltage and (b) scanning speed. Gray and white symbols correspond to cantilevers with contact lengths of 2.5 and 2.2 μm, respectively.

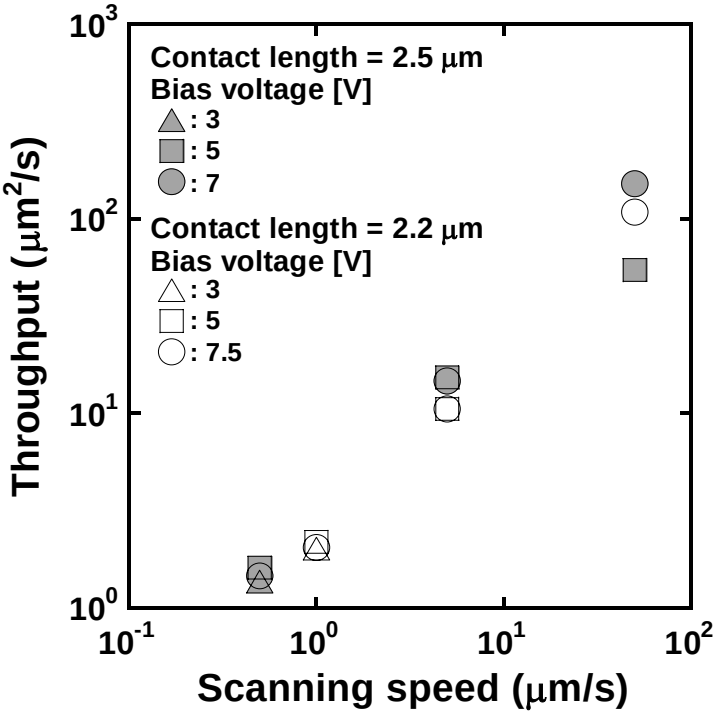


Fig. 3.19 Throughput dependence of the Si oxide on scanning speed of cantilever. Gray and white symbols correspond to cantilevers with contact lengths of 2.5 and 2.2 μm, respectively.

Furthermore, in order to realize large-scale oxidation, an SPM tip with a contact length of 15 μm was prepared by focused-ion-beam (FIB) etching, as shown in Fig. 3.20(a). The cantilever was tilted about 13° during FIB etching, in order to adjust the etched surface of the SPM tip to the mounting angle of the cantilever holder. From this, the etched surface of the tip makes extensive contact with the sample surface. The scan direction is also shown in Fig. 3.20(b). In addition, experiments were carried out using the SPM tips with contact length of 5.9 and 8.3 μm in order to investigate the size dependence of the oxide region on the contact length of the SPM tip. Here, the width and height of the Si oxide were measured by using a Si_3N_4 tip with a tip radius of 15 nm.

Figure 3.21 shows scanning SEM images of the SPM tips and the Si oxide structures in large-scale SPM local oxidation under different conditions. By increasing the contact length of the tip from 5.9 to 15 μm, the width of the fabricated Si oxide grows from 5.4 to 11.4 μm. This result suggests that the width of the Si oxide is almost determined by the contact length of the SPM tip. On the other hand, Fig. 3.21 also exhibits that the height of the Si oxide are estimated to be about 0.6 and 2 nm with the applied bias voltage of 5 and 50 V, respectively. The height of the 11.4 μm Si oxide is not obtained because the size of the oxide is too large to measure by our SPM system. However, from the similarity of the oxidation conditions between the 6.1 μm oxide and the 11.4 μm oxide, it is suspected that the height of the 11.4 μm oxide is approximately 2 nm.

Furthermore, we investigate the influence of the contact force on the size of micrometer-scale Si oxide using the SPM tip with a contact length of 15 μm. Figure 3.22 shows SEM images of 10 micrometer-scale oxide formation performed at various contact forces ranging from 0.1 to 2.1 μN with the DC voltage of 50 V. A visual inspection reveals that the size uniformity of the Si oxide is strongly dependent on the contact force and the vertical growth rate is suppressed with the increase of the scanning speed at low contact

forces. In particular, the Si oxide has poor uniformity at low contact forces below 1.3 μN with a high scanning speed of 200 μm/s. On the other hand, at high contact forces above 1.5 μN, the Si oxide with good size uniformity is obtained even with a high scanning speed of 200 μm/s. This result indicates the threshold contact force for Si oxide formation with good size uniformity is about 1.5 μN. In addition, the width dependences of the Si oxide region on the contact force and scanning speed of the SPM tip are shown in Figs. 3.23(a) and (b), respectively. As shown in these figures, the Si oxide region over 11 μm width is produced by the SPM tip with the contact length of 15 μm. The width of Si oxide is not affected by the contact force and scanning speed. These results show the width of the Si oxide is determined by the contact length of the SPM tip. Since the local oxidation occurs within the water meniscus, the width of the Si oxide is strongly affected by the contact length of the SPM tip. Moreover, the height of the Si oxide depends on the electric field strength between the SPM tip and sample surface, and the growth rate of the Si oxide increases with the electric field [24]. It is also considered that the average distance between the etched surface of the SPM tip and the sample surface depends on the contact force. At higher contact forces, the etched surface of the SPM tip comes close to the sample surface. Therefore, the intensity of electric field across the tip and the sample is stronger than at lower contact forces. Hence, the growth rate of the Si oxide enhances with increasing the contact force of the SPM tip, resulting in the formation of the Si oxide with good size uniformity even at high scanning speed. Thus, it is possible to improve the uniformity of the fabricated Si oxide with the control of the contact force. These results imply that higher contact forces are important for high-speed 10 micrometer-scale SPM local oxidation.

Figures 3.24(a) and (b) show the throughput, which is defined as the oxide area divided by the writing time, as a function of the contact force and scanning speed, respectively. As shown in Fig. 3.24(a), the throughput does not depend on the contact force. On the other hand,

Fig. 3.24(b) exhibits that the throughput increases almost linearly with the scanning speed. This is due to the fact that the width of the Si oxide region is dominantly controlled by the contact length of the SPM tip. Moreover, when the local oxidation conditions were 1.5 μN and 200 μm/s, the throughput of Si local oxidation reached about 10^3 $\mu m^2/s$, which is 10^5 times larger than that of conventional SPM local oxidation. These results imply that high-speed, 10 micrometer-scale SPM local oxidation is realized with a SPM tip having 10 micrometer-scale contact length.

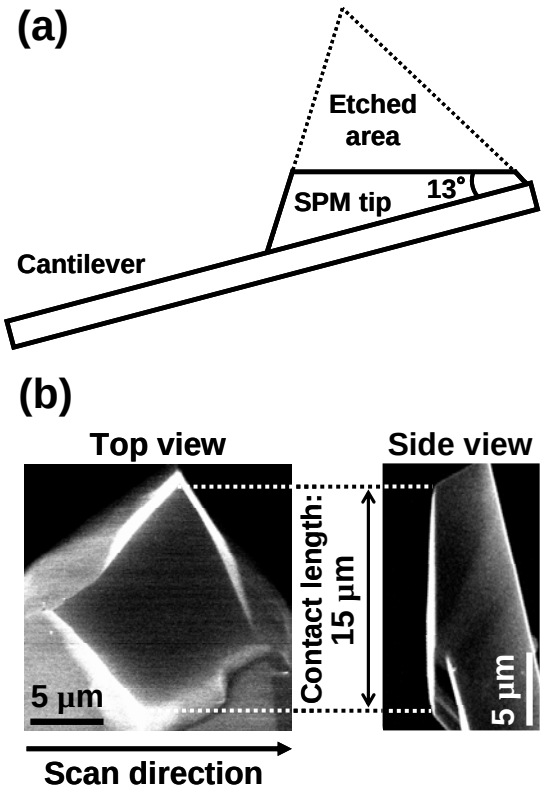


Fig. 3.20 (a) Schematic representation of SPM cantilever with a fabricated tip obtained by FIB etching. (b) SEM images of SPM tip used for 10 micrometer-scale SPM local oxidation.

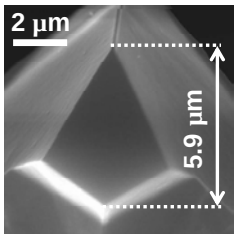
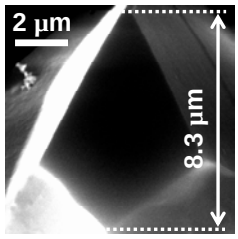
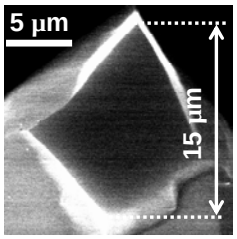
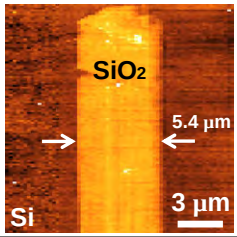
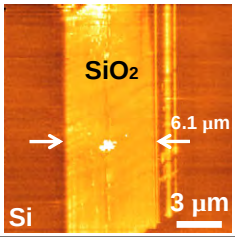
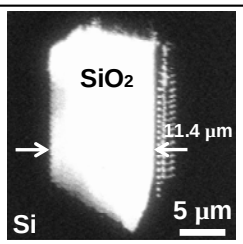
Images of SPM tip	**SEM image**		
			
Contact length	**5.9 µm**	**8.3 µm**	**15 µm**
Images of Si oxide	**SPM image**		**SEM image**
			
Bias voltage [V]	**5**	**50**	**50**
Scanning speed [µm/s]	**0.5**	**10**	**10**
Contact force [µN]	**2.8**	**1.5**	**1.5**
Width [µm]	**5.4**	**6.1**	**11.4**
Height [nm]	**0.6**	**2**	**——**

Fig. 3.21 SPM tips and Si oxide structures of 10 micrometer-scale SPM local oxidation performed for different oxidation parameters.

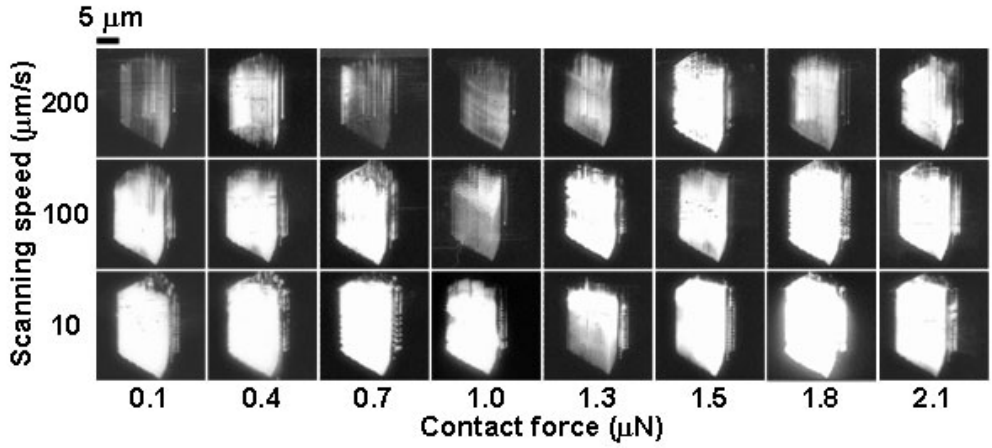


Fig. 3.22 SEM images of 10 micrometer-scale Si oxide fabricated by different scanning speeds and contact forces. DC voltage was set at 50 V. Contact length of the tip was 15 μm.

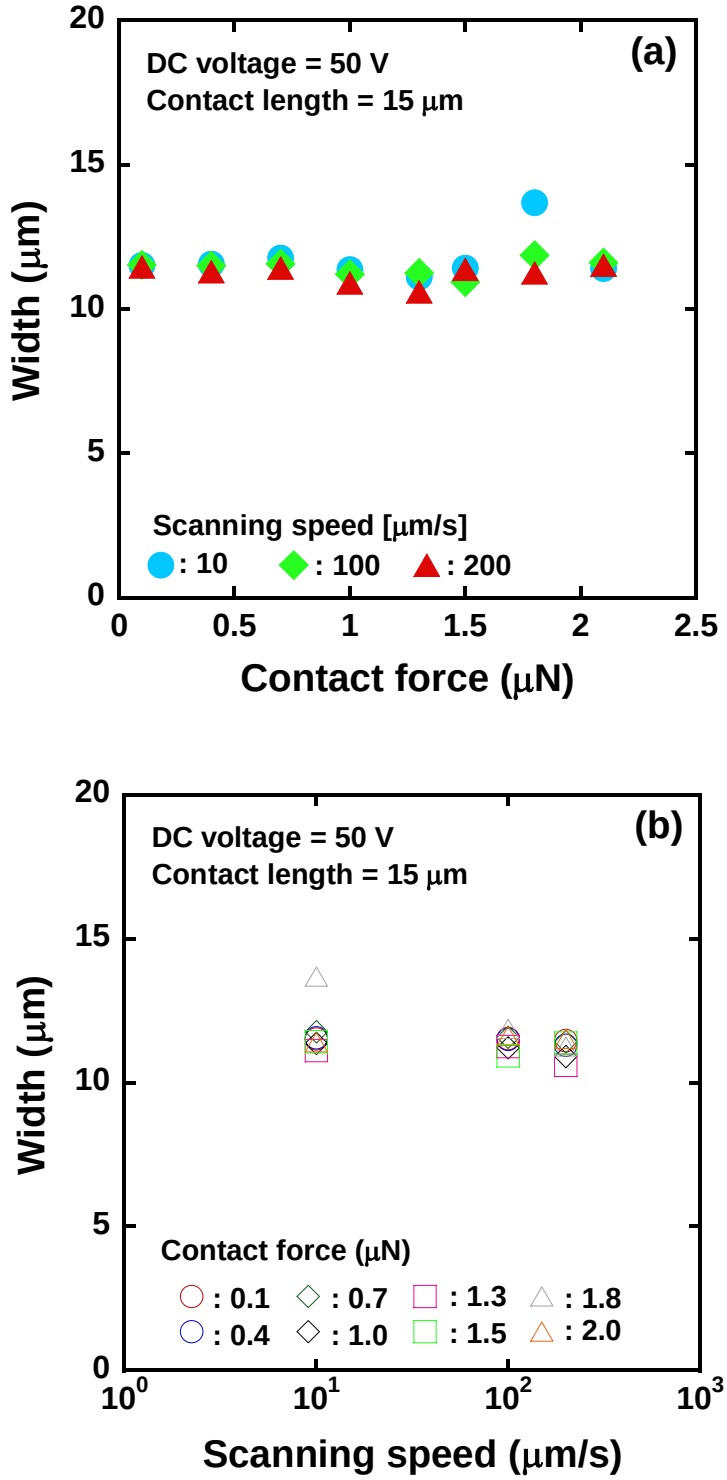


Fig. 3.23 Width dependences of 10 micrometer-scale Si oxide on (a) contact force and (b) scanning speed of the SPM tip.

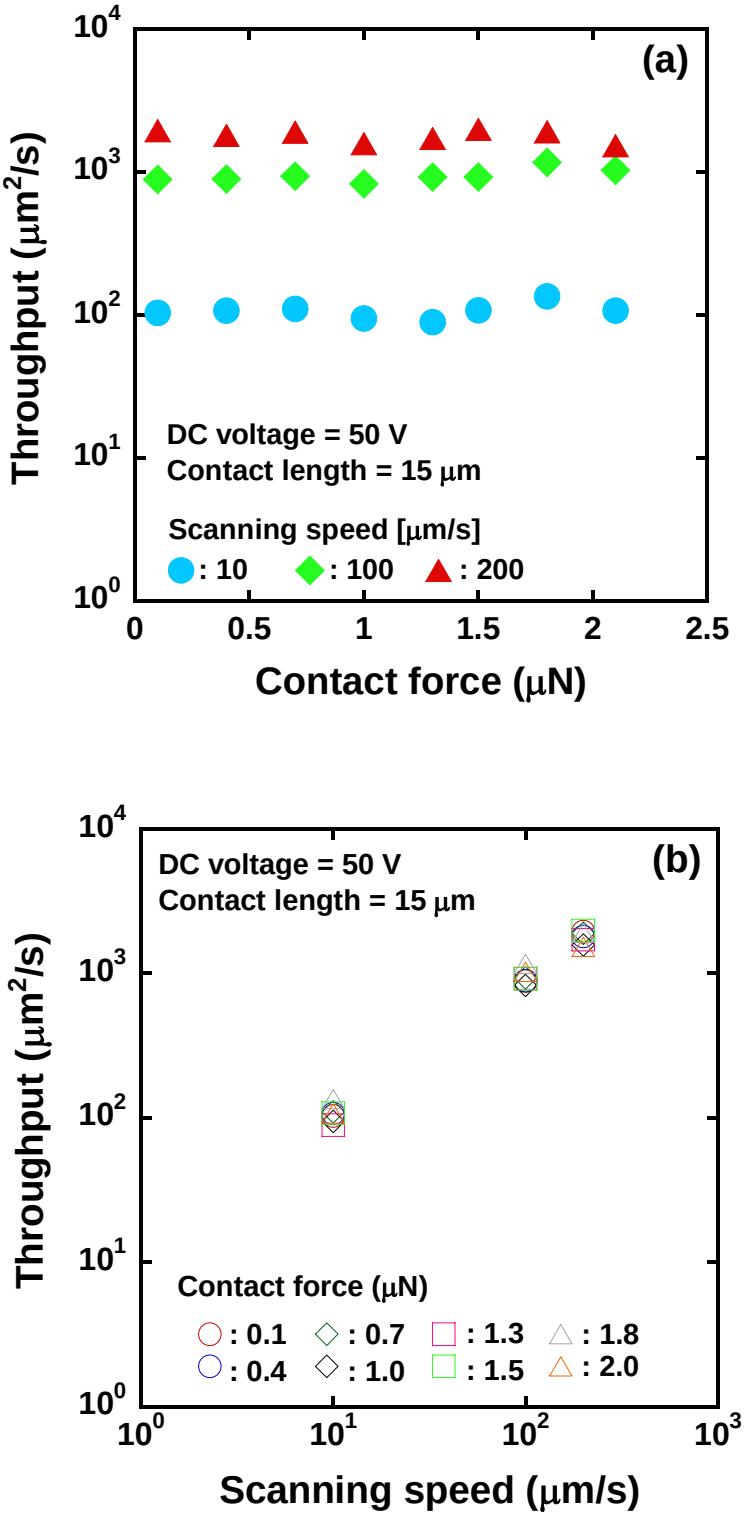


Fig. 3.24 Throughput dependences of 10 micrometer-scale Si oxide on (a) contact force and (b) scanning speed of the SPM tip.

3.5 Summary

In conclusion, the nanometer-scale modification of Si surfaces is demonstrated by active control of the cantilever dynamics in tapping-mode SPM local oxidation. The feature size of Si oxide wires was well controlled by varying the oscillation amplitude and Q-factor of the cantilever. The size controllability of the Si oxide was more strongly affected by the oscillation amplitude of the cantilever than the Q-factor. By optimizing the control parameters such as applied bias voltage to the tip, scanning speed of the tip and oscillation amplitude of the cantilever, the fabrication of Si oxide wires with sub-10 nm dimensions was achieved. The average width and minimum FWHM of the Si oxide wire were 9.8 nm and 8.5 nm, respectively. Furthermore, the STD of the fabricated oxide was measured to be around 2-3 nm in width and 0.1-0.2 nm in height in spite of the active control of the cantilever dynamics.

Furthermore, we exhibited the model of tapping mode SPM local oxidation based on the oxidation ratio and the rate constant. From the model, the oxidation ratio is estimated to be 10-16 % in tapping mode oxidation with 10 nm resolution. The rate constants of tapping mode oxidation are larger than those of contact mode oxidation, which suggests the formation of small and uniform oxide in tapping mode operation. These results imply that tapping mode SPM local oxidation is a suitable technique for the fabrication of nanometer-scale Si oxide wires with higher controllability and better size uniformity.

On the other hand, we demonstrated 10 micrometer-scale SPM local oxidation on a Si surface with a SPM tip having a large contact length. The width of the Si oxide depends on the contact length of the SPM tip with the sample surface. We also investigated the influence of contact force on the size of Si oxide. The Si oxide with good size uniformity was obtained with a high scanning speed of 200 μm/s at high contact forces above 1.5 μN. Thus, not only the contact length of the SPM tip but also the contact force is important for 10 micrometer-scale SPM local oxidation lithography. Furthermore, the throughput of 10

micrometer-scale SPM local oxidation was enhanced almost linearly with the scanning speed, and reached about 10^3 $\mu m^2/s$, which is about 10^5 times larger than that of conventional SPM local oxidation. These results suggest that this method could be a key technique for the fabrication of nanometer-scale devices with micrometer-scale dimensions.

Chapter 4

Scratch Nanolithography Using Scanning Probe Microscopy

4.1 Introduction

Scanning probe microscopy (SPM) systems, such as atomic force microscopy (AFM) and scanning tunneling microscopy (STM), are not only useful for the evaluation of surfaces, but are also promising candidates for nanolithographic tools because of their operational versatility and simplicity. One interesting and promising method using SPM-based nanolithography techniques is not only anodic oxidation between SPM tip and sample surface but also the mechanical scratching of surfaces with a SPM tip [1, 2]. The sufficiently high force between the SPM tip and the substrate surface can lead to the removal of materials and fabricate grooves on the substrate. Direct patterning attracts a great deal of interest because no further processing step is required.

In this dissertation, we investigate the sub-20 nm nanolithography on Si using SPM scratching with a diamond-coated SPM tip. Furthermore, the groove size dependence of Si on various scan parameters such as applied force, scanning speed and number of scan cycle are also studied.

4.2 SPM Scratch Nanolithography

In SPM scratch nanolithography, materials can be removed from the surface of the sample by applying the SPM tip with a sufficient force, and then grooves can be produced. SPM scratching is regarded as a direct patterning and resistless lithography method, where a tip is used to provide local friction on the sample to modify the surface. Figure 4.1 shows the schematic diagram of scratching using an AFM. SPM scratching has become an attractive method because it can be used to process not only metals [3, 4] and semiconductors [5, 6] but also insulators [1, 2, 7], and it does not need a bias voltage for lithography. Recently, Hyon et al. reported that they mechanically patterned a groove with a width of 7 nm on GaAs surfaces [6]. On soft materials, it is possible to perform nanometer scratching using a Si or Si_3N_4 tip with a radius of less than 20 nm. In contrast, on hard materials such Si, a diamond tip with extremely high wear resistance should be used [8-14]. The radius of the diamond tip is generally larger than the tip used for soft materials because of the polycrystalline diamond coating on the tip-side of the Si cantilever. Since SPM scratching on Si is usually performed in a high-force regime (from approximately 10 μN to mN), sub-20 nm nanolithography of Si using SPM scratching has not yet been reported.

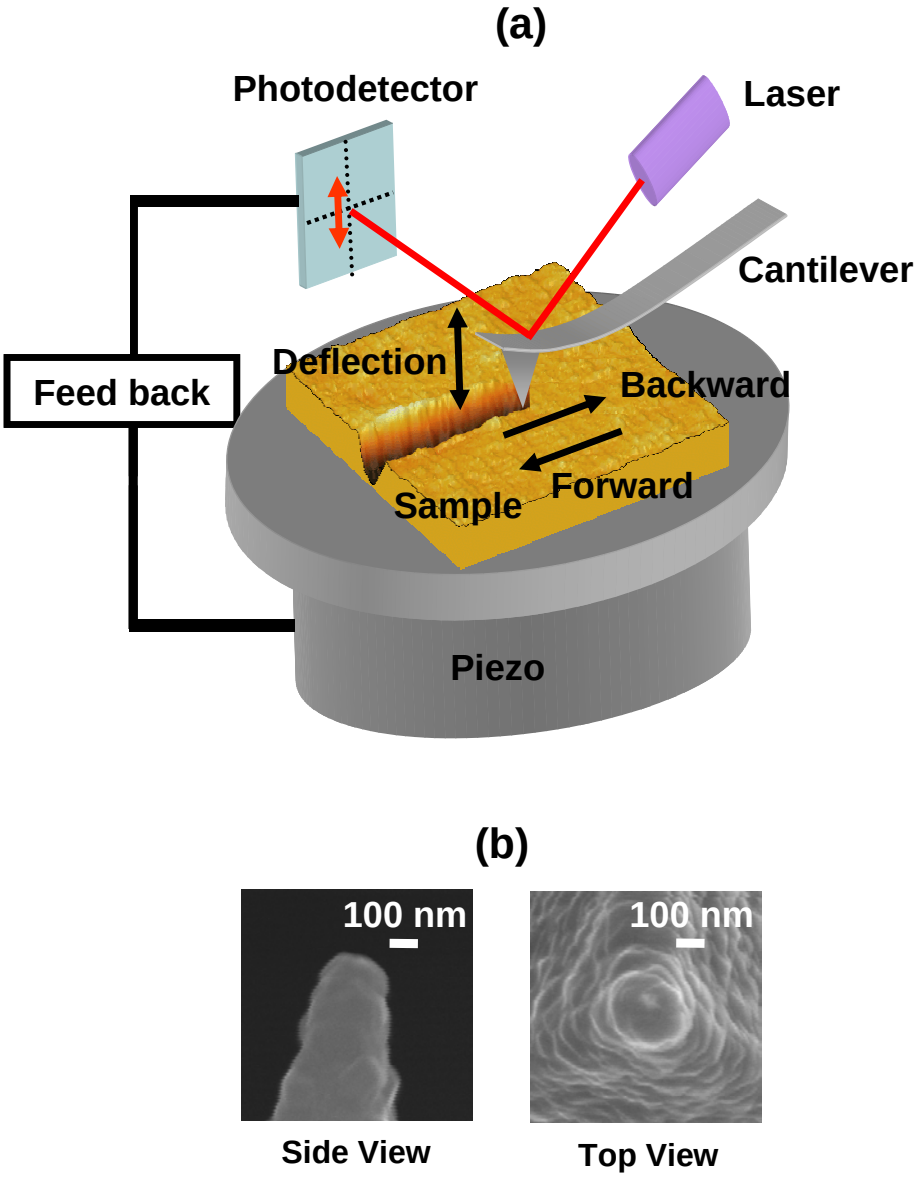


Fig. 4.1. (a) The schematic diagram of scratching using an AFM. (b) SEM images of a diamond-coated SPM tip (side and top view).

4.3 Size Dependence of Si on Various Scan Parameters

In SPM scratching nanolithography, we use a contact mode AFM to mechanically modify the surfaces of Si and investigate the scratching properties of Si on several scanning parameters such as applied force, number of scan cycles, and scan speed.

The experiments were performed in ambient conditions using an AFM system (SPI4000 and SPA400, SII NanoTechnology). The sample was cut from a wafer of p-type Si (100). The silicon surface was preliminary cleaned by sonication in organic solvents and rinsed with pure water, then the samples were dipped in HF (10 %) for 1 minute to remove the native oxide layer. The centerline average roughness (R_a) and the maximum roughness (R_{max}) of the sample surfaces measured from 1.0×1.0 μm^2 topographic AFM images were less than 0.08 nm and 0.3-0.5 nm, respectively. For scratching, a diamond-coated tip with spring constant of 45 N/m was used, as shown in Fig. 4.1(b). The thickness of the diamond layer was about 100 nm and the tip radius was in the range between 100 and 200 nm. The normal force was calculated using Hooke's law from the cantilever deflection and spring constant. The applied force varied from 1 to 9 μN. After scratching, the samples were dipped again in HF (10 %) to remove any oxide that may have been formed during the scratching process. Observation of the grooves was conducted using a Si_3N_4 tip with spring constant of about 0.02 N/m. SPM scanning was realized along one direction only, forward and backward along the same path. Scratching was performed using a vector scan method.

Figure 4.2(a) shows an AFM image of five scratches generated at various forces (from left to right: 1, 3, 5, 7, and 9 μN) and a scanning speed of 10 nm/s on a Si(100) surface. The scratches were performed by one scan cycle in the forward direction. The groove with the width of a few tens of nanometers was obtained. It is considered that sharp edges of single-crystal diamond grains at the very end of the tip play an important role in the resolution of scratch nanolithography at low force regime below 9 μN. Figure 4.2(b) also shows a

cross-sectional profile of the grooves, taken along the white line, shown in Fig. 4.2(a). As expected, the groove size increases with the normal applied force. It was found that wear debris sediments tend to accumulate around the grooves. The level of protuberance along the grooves, which is induced by contact stress, also increased with the applied force.

The variation in the groove size at various scan parameters is shown in figures 4.3 (a)-(c). The width and depth of the grooves were measured from the groove profiles, 10 points per groove, and then averaged. The line width of the grooves is defined by the full width at half maximum (FWHM). Figure 4.3(a) shows the width and depth of the grooves as function of the applied force in the forward and backward directions. The groove formed at the applied force of 1 μN in the backward direction was not measured because the groove size was comparable with surface roughness. The results show that the width and depth increase linearly with the applied force. The minimum groove width of 10 nm was successfully patterned on Si surfaces by SPM scratching. It can be seen that the groove size was different with the scan direction. This result may be caused by the surface orientation states induced by the single-crystal diamond grains on the tip. Figure 4.3(b) shows the width and depth of the grooves as function of the number of scan cycles. Scratching was performed at the applied force of 9 μN and scan speed of 10 nm/s in the forward scan. As expected, the groove size increases with the number of scan cycles. The size of the grooves ranges from about 20 nm to 25 nm in width and about 2.5 nm to 6.5 nm in depth. It seems that the scratching mechanism of the Si atoms is layer-by-layer removal [9, 12-14]. The width and depth of the grooves are plotted as function of the scan speed in figure 4.3(c). The grooves were generated by one scan cycle in the forward direction at scan speeds of 0.01-10 μm/s and an applied force of 9 μN. The width and depth of the grooves were almost constant at given scan parameters. Therefore, the size of the grooves no longer depends on the scan speed. The groove patterns with controlled width and depth could be achieved by adjusting the applied force, scan direction

and the number of scan cycles. Furthermore, no deterioration of the tip was observed after 10 μm/s scratching. It is concluded that the high speed nanolithography can be achieved without degradation of the patterns by SPM scratching.

As shown in Fig. 4.2(a), there are fluctuations in the size of the grooves. Therefore, we have determined the standard deviation (STD) of the width and the depth from ten cross sections across the grooves. The size fluctuation of the groove formed at 1 μN is shown in Fig. 4.4. The fabricated groove is uniform compared with the surface roughness. The STDs of the width and depth were determined to be 1.09 and 0.04 nm, respectively. This suggests that the applied force during scratching is precisely controlled using an optical beam deflection AFM system. Hence, the size fluctuation of this groove can be suppressed considerably. Figure 4.5(a) shows the relationship between the STD of the groove size and a normal force. The amounts of fluctuation in the width and depth increase as normal force increases. The maximum STD was obtained to be 2.0 nm in width and 0.3 nm in depth under an applied force of 9 μN. Figure 4.5(b) shows the relative STDs (RSDs). RSD, which is defined as the ratio of STD to the corresponding average size, ranged from 7.4 to 11.0% and became less dependent on the normal applied force. In other words, the fluctuation in the average size is almost constant. A similar behavior is also seen in patterned width of GaAs grooves with RSDs of 13-17% [6]. Therefore, it is possible that the size fluctuation of the grooves could be controlled at approximately 10% without depending on the applied force.

Here, the wear coefficient is known as an important wear parameter. The wear coefficient of Si(100) was calculated using Archard's wear law [15], which is generally utilized for the quantification of wear. Archard's wear law is given by

$$V = k \frac{L\,S}{H}, \tag{4.1}$$

where V is the volume loss of a material caused by wear, L is the normal force, S is the sliding distance, H is the hardness of the worn material, and k is the dimensionless wear

coefficient. By measuring the volume of the material removed, the wear coefficient was assessed. The wear volume and wear coefficient are shown in Fig. 4.6. As expected, the wear volume substantially increased as the applied force increased. The result showed that the wear coefficient of Si(100) ranged from 0.05 to 0.09. Furthermore, this is in agreement with the data compiled from the experimental results of pin-on-disk and AFM tests on Si materials [16, 17].

Next, more complex nanostructures were realized using SPM scratching. By optimizing these scan parameters, the line and space patterns were formed on Si surfaces and are shown in figures 4.7 (a)-(e). The line and space patterns were adjusted from 100 nm to 30 nm pitch conditions. The results show that the line and space patterns were not degraded and were patterned clearly with their conditions. When the applied force, scan speed, scan direction, and the number of scan cycles were set at 9 μN, 10 μm/s, backward, and one cycle, respectively, 30 nm pitch line and space patterns could be realized. Figure 4.8 shows an AFM image of a dot array patterned on Si. The dot diameter is around 40 nm. Furthermore, the dot density measured from AFM images is about $2.6 \times 10^{10}\,cm^{-2}$. Thus, we successfully fabricated a high-density Si quantum dot array using mechanical patterning.

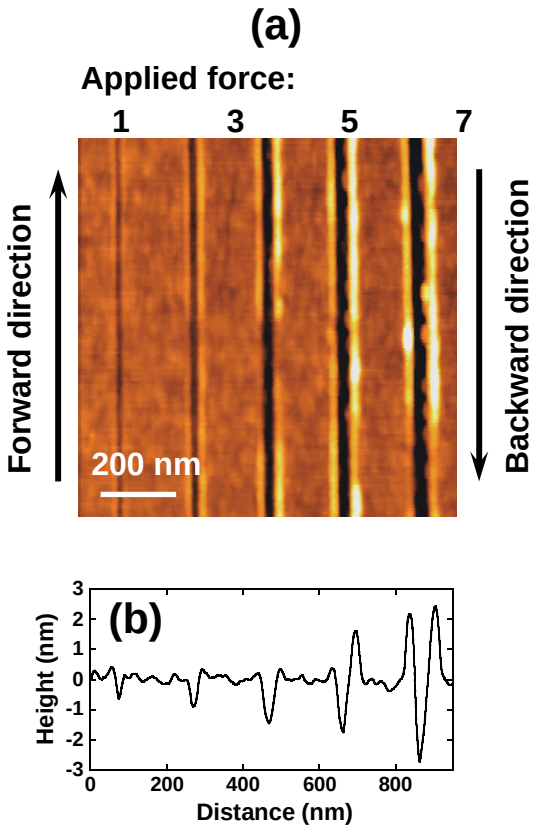


Fig. 4.2. (a) AFM image (1×1 μm^2) of scratched Si(100) surface. The normal applied force varies from left to right as follows: 1, 3, 5, 7, and 9 μN. Grooves were fabricated by one scan cycle in the forward direction. Several different forces were applied with a scan speed of 10 nm/s. (b) Cross-sectional profile along white line in (a).

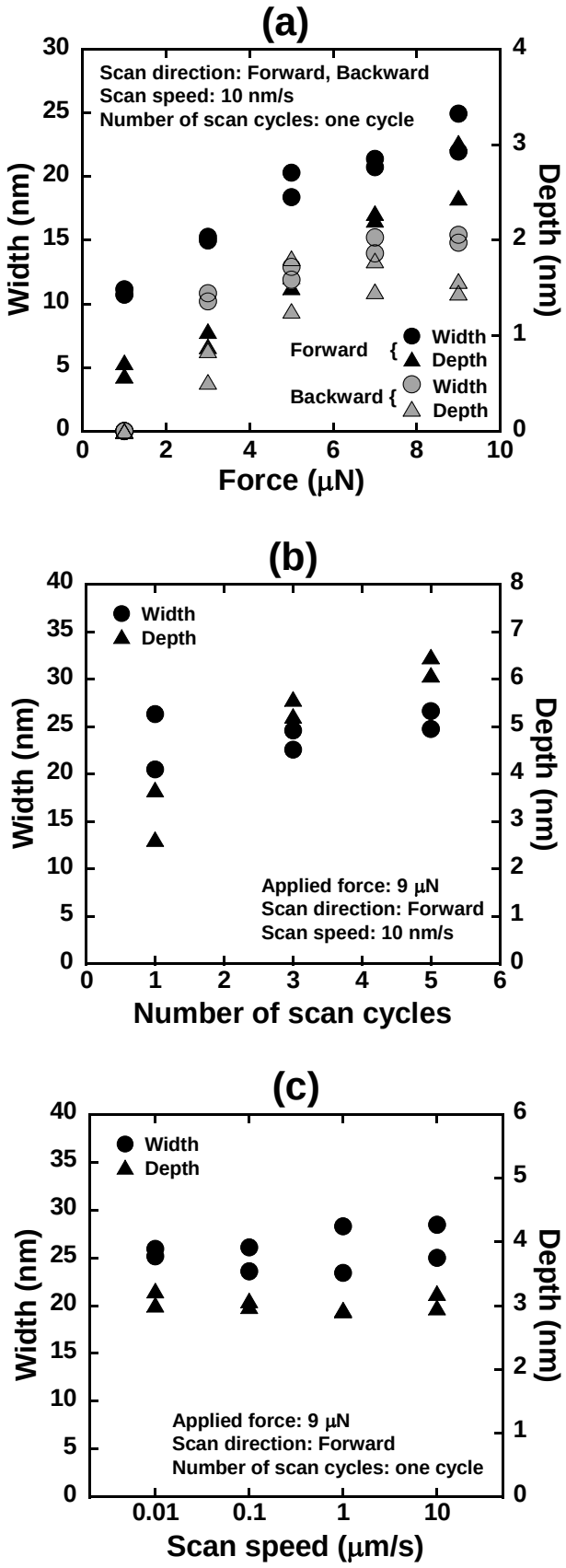


Fig. 4.3. Dependence of groove size on (a) normal applied force, (b) number of scan cycles and (c) scan speed.

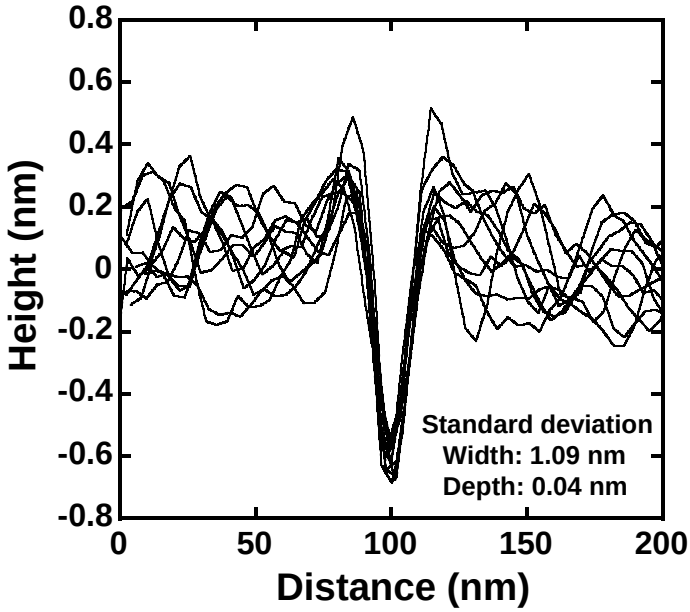


Fig. 4.4. Cross-sectional profiles were taken at 10 points across the groove with a force of 1 μN.

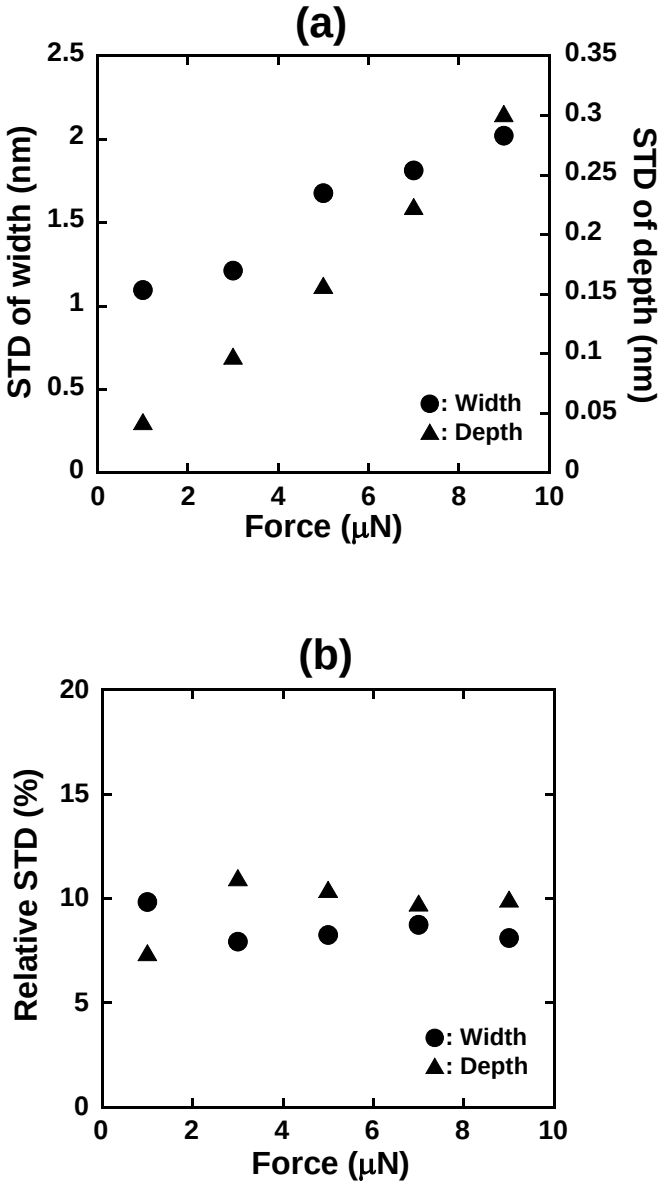


Fig. 4.5. (a) Relationship between normal applied force and STD. (b) Relationship between normal applied force and RSD.

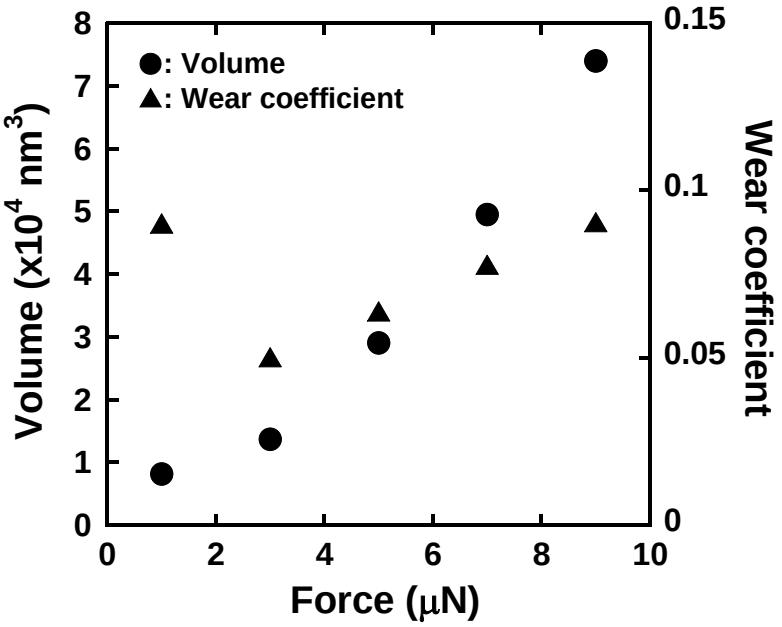


Fig. 4.6. Wear volume and wear coefficient of Si as function of normal applied force.

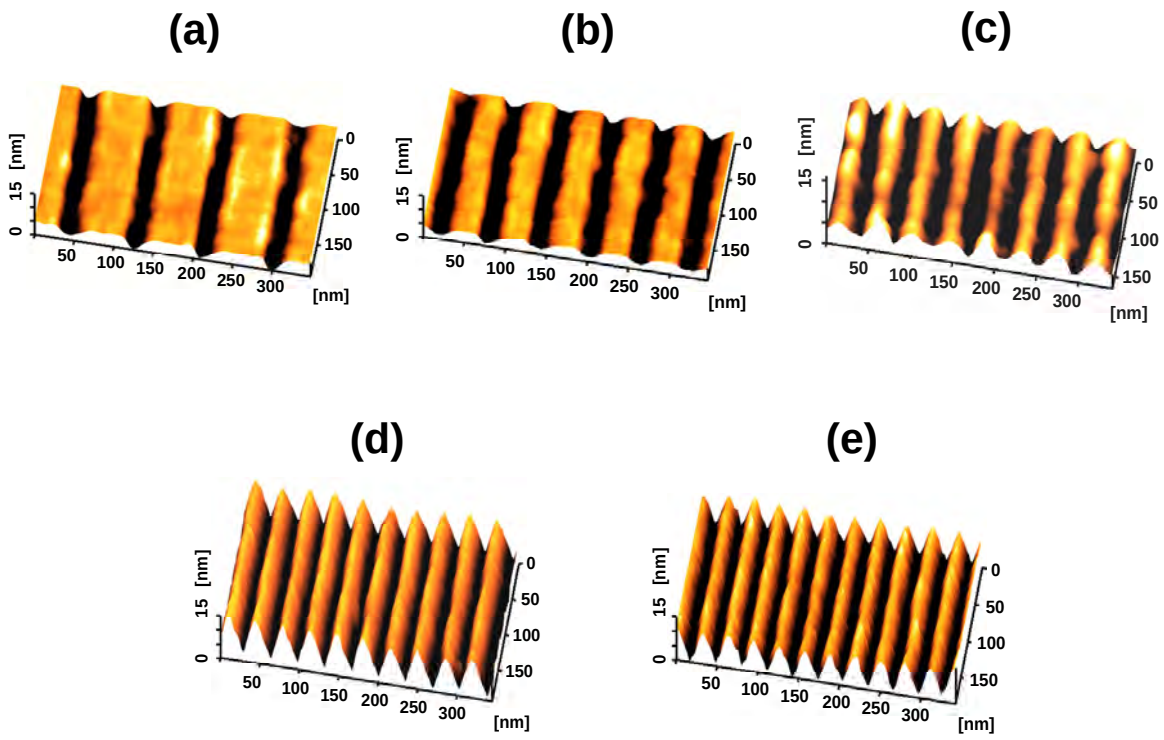


Fig. 4.7. AFM images of line and space patterns with pitch of (a) 100 nm, (b) 70 nm, (c) 50 nm, (d) 40 nm and (e) 30 nm fabricated on Si surface using SPM scratching.

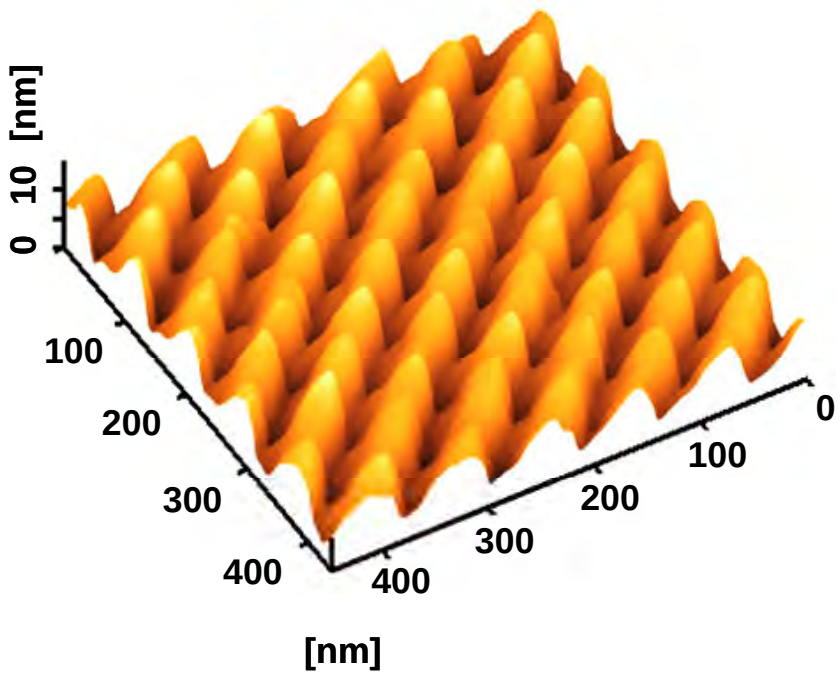


Fig. 4.8. AFM image of quantum dot arrays with 2.6×10^{10} cm^{-2} density fabricated on Si surface using SPM scratching.

4.4 Summary

In a simple and reliable technique for nanoscale patterning of Si surface using SPM scratching with a diamond-coated tip was performed. The influence of scan parameters on groove size was systematically investigated. The groove size was precisely controlled by the applied force, scan direction and scan cycle. The minimum width of 10 nm was obtained on Si surfaces. There was no effect of the scan speed on the groove size. These results show the possibility of high speed nanolithography on Si surface using SPM scratching. Furthermore, the line and space patterns with a pitch of 30 nm and dot arrays with a density of 2.6×10^{10} cm^{-2} were successfully fabricated. Thus, nanoscale mechanical patterning of Si surface could be realized using SPM. The results imply that SPM scratching with a diamond tip allows nanoscale patterning of Si surface to be performed simply, and is particularly well suited for the fabrication of nanoscale devices such as single-electron transistors, quantum computing elements and nanophotonic devices.

Chapter 5

Si Nanoscale Devices Fabricated by SPM Lithography Techniques

5.1 Introduction

Recent progress in nanofabrication technology has provided easy access to smaller dimensions. The promising technologies using scanning probe microscopy (SPM) have been developed and have produced nanoscale devices such as planar-type ferromagnetic tunnel junctions [1, 2], single-electron transistors [3], and superconducting devices [4]. In SPM scratch nanolithography, the tip is scanned under strong loading forces to remove the materials of the surfaces [5, 6]. The advantages of applying SPM scratching for nanolithography are obviously the precision of alignment, the nondamaging definition processes, and the absence of additional etching procedures. In particular, atomic force microscope (AFM) lithography is very promising since AFM is not restricted to conducting materials. SPM scratching has fabricated a variety of structures including holes, grooves, and square areas on metals, semiconductors, and insulators [7-9]. We have recently reported that it is possible to perform sub-20 nm scratch nanolithography on Si with a diamond-coated tip at applied forces less than 9 μN [10, 11].

In this dissertation, SPM scratching is applied to Si nanochannels for the fabrication of Si nanoconstrictions. Electrical and structural properties of Si nanochannels are directly modulated by performing the SPM scratching and are studied from the point of view of nanodevice fabrication. Furthermore, we use a contact mode AFM to mechanically modify the surfaces of Au and investigate the control of conductance of Au at quantum states. In addition, SPM scratching is applied to Si channels for the investigation of magnetoresistive effects in planar-type Si devices.

5.2 Control of Device Properties of Planar-Type Si Devices Using SPM Scratch Nanolithography

SPM scratching nanolithography was applied to Si nanochannels for control of device properties of planar-type Si devices as shown in Fig. 5.1(a) and (b). The starting SOI substrate in this study consisted of 200 nm Si layer and 400 nm buried oxide (box) layer. The top layer is n-type silicon with a resistivity of about 10 Ω·cm. Drain and gate contacts (Ni/Ti/Au = 25/5/35 nm) were defined by electron beam lithography and lift-off process. Figure 5.2(a) also shows the initial AFM image of planar-type Si devices before scratching the Si nanochannel. The current-voltage (I-V) characteristics were measured at 300 K. A typical gate-modulated n-channel MOSFET behavior is observed, as shown in Fig. 5.2(b).

The scratch nanolithography was performed to the Si channel with the applied force of 9 μN, the scan speed of 100 nm/s using a diamond-coated tip in the ambient air. The three times scratching are applied to the Si nanochannel. First, the number of scan cycle is set at 10 cycles. Then, 5 cycles are performed in the second scratching. Finally, 5 cycles scratching is also applied to the Si nanochannel. Here, Si nanochannel was observed by tapping mode in order to suppress the damage of the Si surface after the performing the scratching. Figure 5.3(b) shows the each cross-sectional profile after scratching, and cross-sectional profiles are taken along the line A-B in Fig. 5.3(a). The each drain current after scratching as a function of drain voltage with the gate voltage of 0 V is also shown in Fig. 5.3(c). Drain current decrease with the increase of the number of scan cycles and electrical properties are well controlled by the SPM scratch nanolithography. It is considered that the drain current after the scratching was clearly suppressed due to the constriction of the cross section of the nanochannel.

Here, the cross sectional-area after scratching is estimated from the Fig. 5.4(a). As shown in figure, cross sectional-area gradually decrease with the increase of the number of scan cycles. Figure 5.4(b) shows the drain current as a function of cross sectional-area after

each scratching at the gate voltage of 0 V and drain voltages of 0.1 V. This result indicate that the drain current decrease with the slope of 1.2×10^4 nm^2/dec. It is concluded that the scratch nanolithography using SPM is useful for the control of the electrical properties in planar-type Si devices.

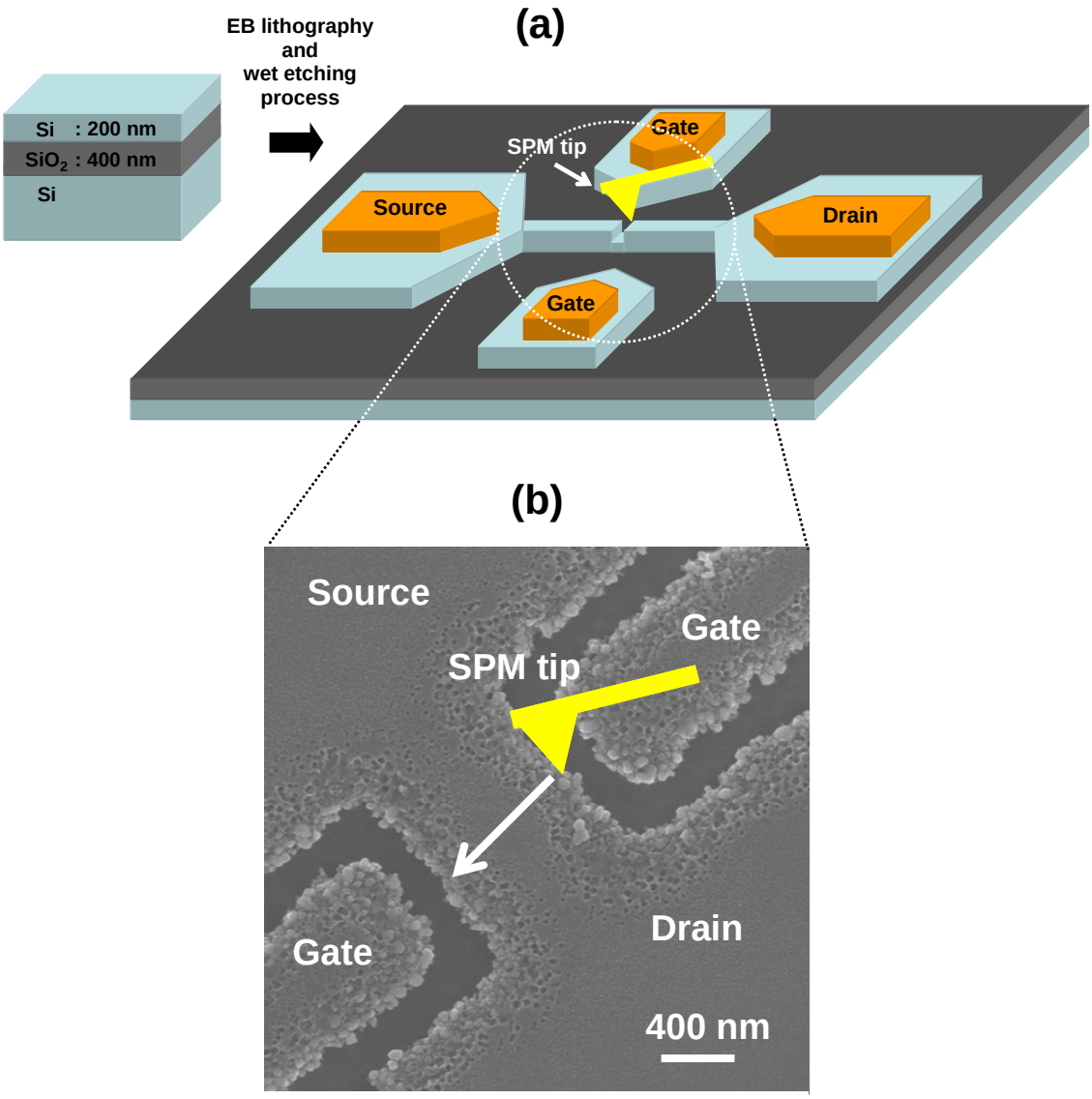


Fig. 5.1. (a) Schematics of planar-type Si devices. (b) SEM image of Si channel and the direction of scratching for the Si channel.

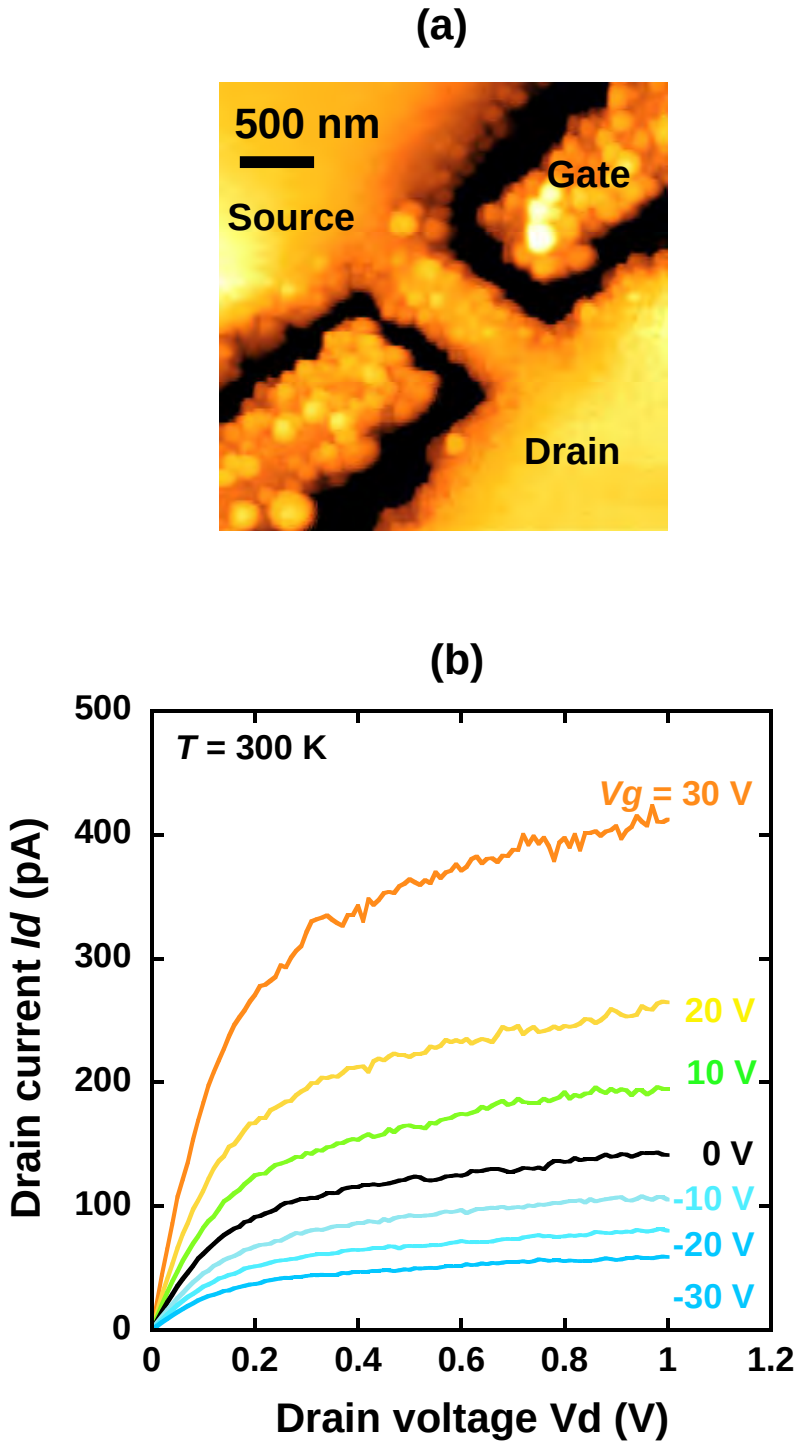


Fig. 5.2. (a) Initial AFM image of planar-type Si devices the Si nanochannel. (b) Current-voltage (I-V) characteristics of planar-type Si devices before scratching.

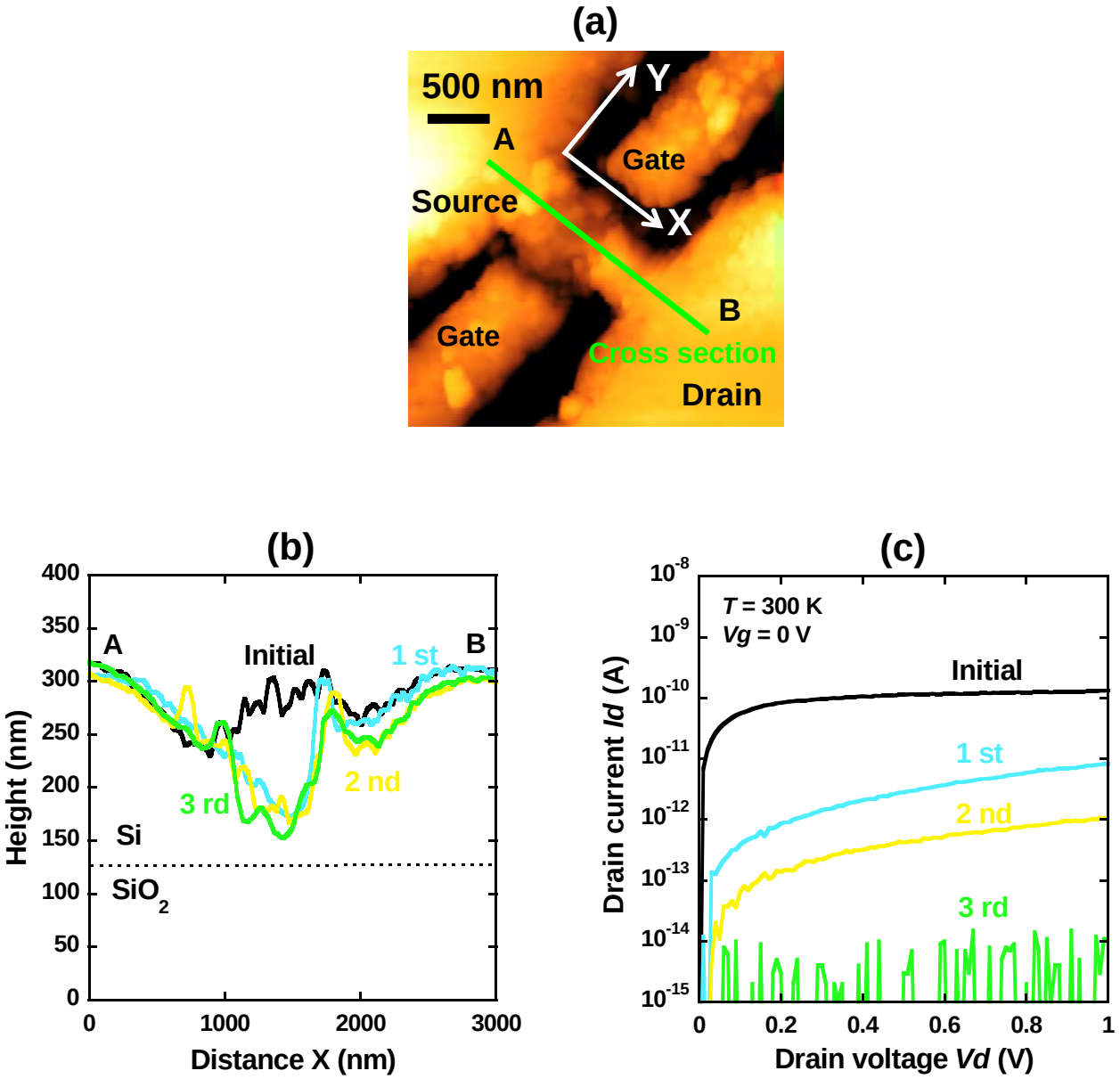


Fig. 5.3. (a) AFM image after third scratching (b) Cross section of Si channel after each scratching. (c) Drain current after scratching as a function of drain voltage with the gate voltage of 0 V at 300 K.

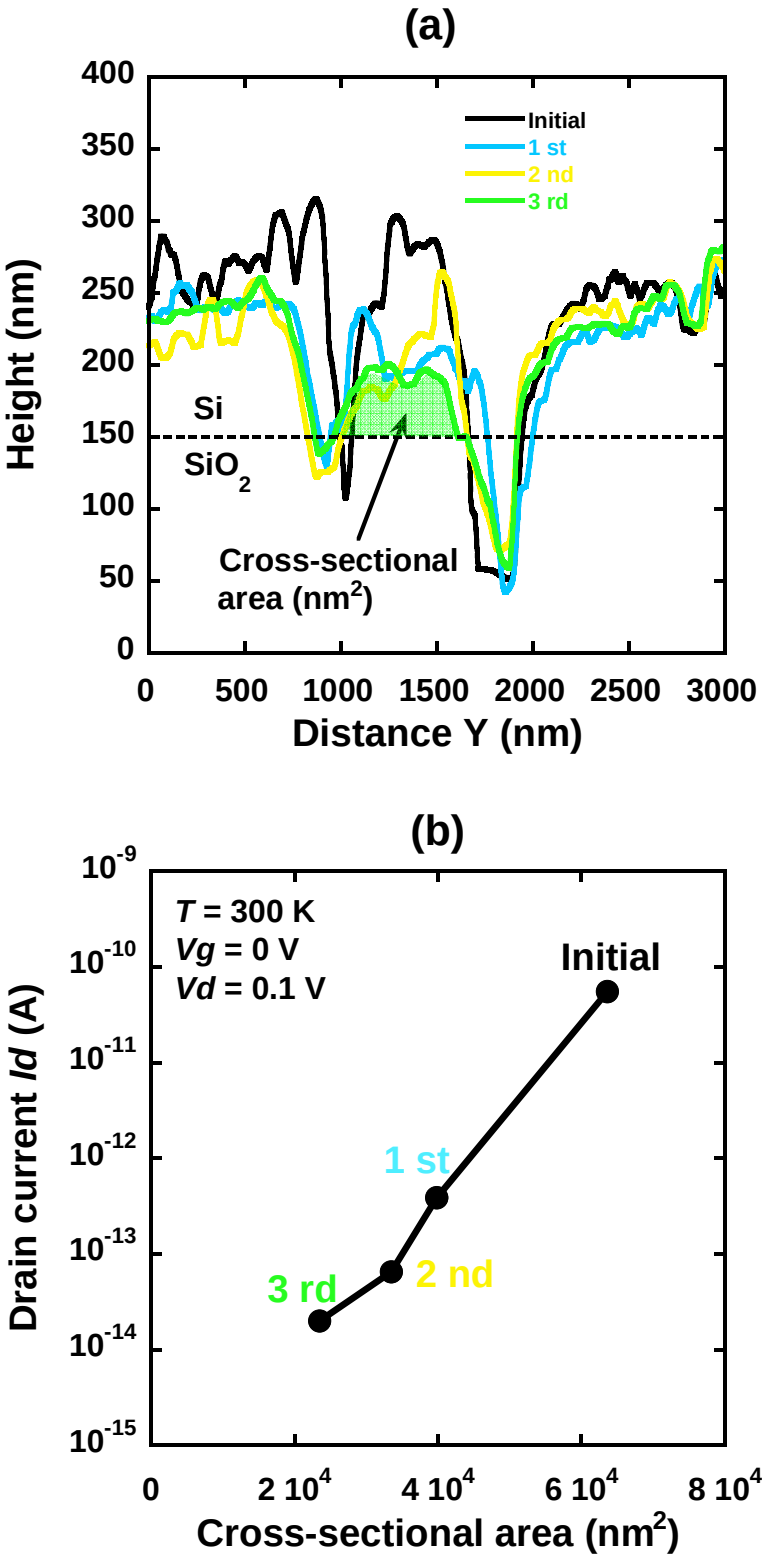


Fig. 5.4. (a) Cross sectional area after scratching. (b) Drain currents as a function of cross sectional-area after scratching.

Moreover, we estimate the bending breaking force for the scratching of Si nanochannels. Figure 5.5(a) shows the AFM image and schematic of the Si nanochannel, respectively. Here, we show the model of SPM scratching based on the bending breaking force. Figure 5.5(a) also shows the schematic illustration of the Si nanochannel. The flexural strength is calculated by the equation,

$$\sigma = \frac{M}{I} \times \frac{a}{2} = \frac{\frac{wc}{4}}{\frac{ba^3}{12}} \times \frac{a}{2} = \times \frac{3wc}{2ba^2}, \tag{5.1}$$

$$w = \frac{2ba^2\sigma}{3c}, \tag{5.2}$$

where M is bending moment, I is geometrical moment of inertia, and σ is flexural strength. The width, height and length of the Si channel are described as the symbol of a, b, and c, respectively. Here, the flexural strength of Si is to be 7.8×10^{-11} N/nm^2. Therefore, we estimate the bending breaking force of Si channel from the equation. As shown in Fig. 5.5(b), the three types of Si channel was prepared and scratching is applied to the samples with the applied force of 9 μN, the scan speed of 100 nm/s and number of 1 scan cycle . Then, all Si channels are removed from the surface. Since the flexural strengths of three sample in Fig. 5.5(b) were identified to be 3 μN, 0.2 μN and 0.4 μN, respectively, the applied force of 9 μN is not suitable for the channel scratching. Furthermore, nine different shapes of Si nanochannels are prepared as shown in Fig. 5.6, which is the cross-sectional area of Si channel versus flexural strength. The height of Si channel is described in the figure. The Si channels with the height of 11, 100, 43, 60 nm are removed from the surface. These results indicate that we can easily estimate the applied force to the Si channel and SPM scratching techniques are useful for the fabrication of planar-type Si devices.

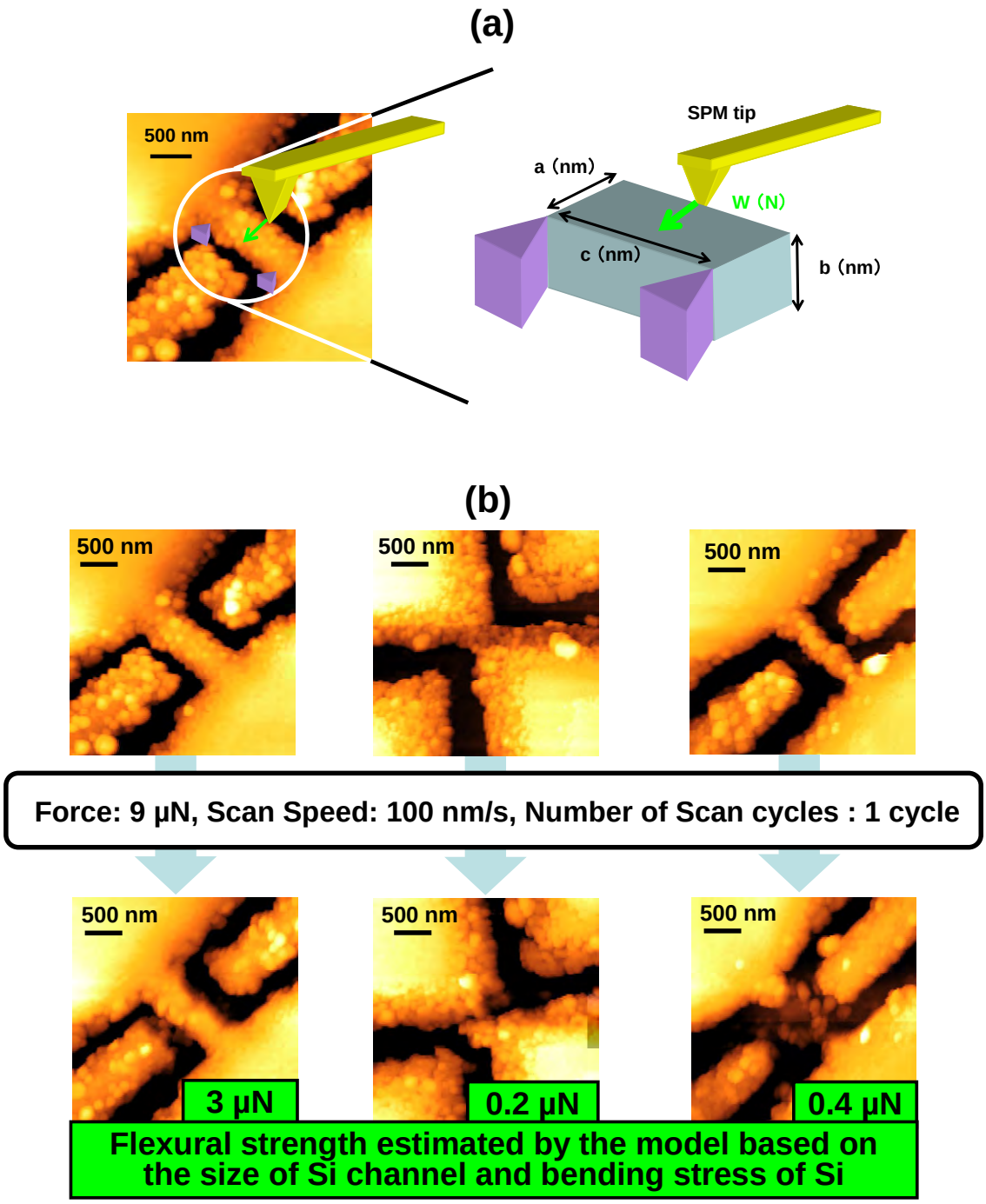


Fig. 5.5. (a) AFM image and schematic of the Si nanochannel. (b) The relationship between the size of channel and flexural strength.

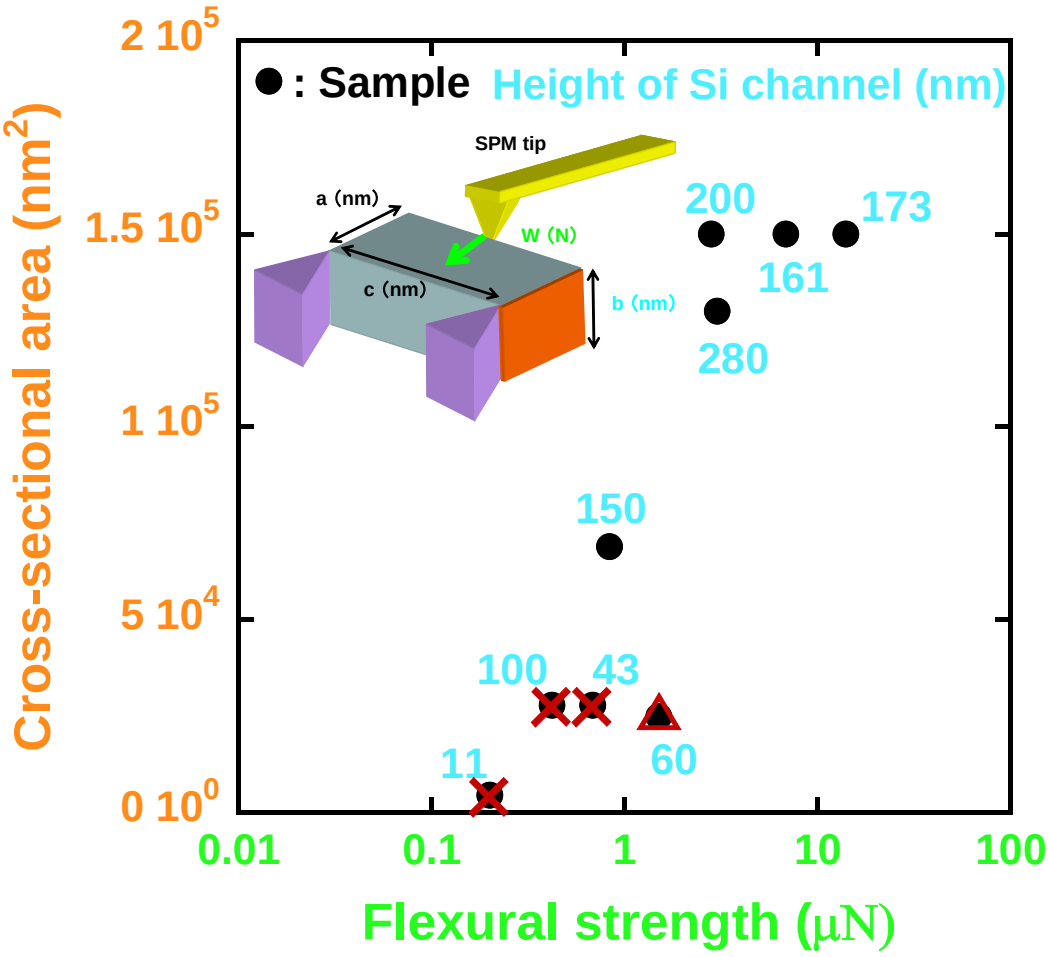


Fig. 5.6. Cross-sectional area as a function of flexural strength at various height of Si channel.

5.3 Control of Quantum States in Au Using SPM Scratch Nanolithography

SPM scratching nanolithography was applied to Au nanochannels for control of device properties of planar-type devices with in-situ measurement as shown in Fig. 5.7(a). The SEM image of diamond coated SPM tip is shown in Fig. 5.7(b). The starting substrate in this study consisted SiO_2/Si as shown in Fig. 5.8. Then, Au channel (Ti/Au = 5/30 nm) were defined by electron beam lithography and lift-off process on the substrate. Figure 5.9 exhibits the experimental set-up and the initial AFM image of planar-type devices before scratching the Au channel. The experiments were measured at 300 K and performed in ambient air. For the measurement of the quantum point contact (QPC) in Au wire with in-situ method, the bias voltage of 10 mV is applied to the sample between source and drain. The observation of groves on Au channel was conducted using Si_3N_4 tip with spring constant of about 0.02 N/m.

Figure 5.10 shows the AFM image of grooves at various directions. Here, it is considered that the sharp edges of single crystal diamond grains at the very end of the tip play an important role of scratch nanolithography. As shown in Fig. 5.10, the diamond coated SPM tip used in this experiment is suitable for the fabrication of nanometerscale grooves with better size uniformity in the forward and up direction. Hence, the scratches for the fabrication of quantum states in Au wires are performed in the forward and up direction.

Figures 5.11 (a) and (b) shows the conductance of Au wire as a function of the time during scratch nanolithography in forward and up directions, respectively. The scanning speed and applied force of the SPM tip is set at 50 pm/s and 18 μN, respectively. The conductance is drastically suppressed at the time of about 1150 s in the forward direction. The conductance in up direction is also suppressed at the time of about 2200 s. The Au channel is broken and insulated in these times by SPM scratching.

Here, Snow et al proposed the rectangular model of resistance modification in Au wires as shown in Fig. 5.12. The resistance of Au channel is expressed as follows,

$$R = \Delta R_{modify}(t) + R_{initial} \tag{5.3}$$

$$\Delta R_{modify}(t) = \rho \frac{L}{T}\left(\frac{1}{\omega_0 - vt} - \frac{1}{\omega_0}\right) \tag{5.4}$$

where R is resistance of Au chnannel, $R_{initial}$ is initial resistance of Au channel before scratching nanolithography, and $\triangle R_{modify}(t)$ is the increase of resistance in Au channel with respect to the time t during scratching nanolithography. The resistivity is described as ρ. The resistivity of Au is generally 2.2×10^{-8} Ωm. The length, width and thickness of the channel are expressed as the symbol of L, ω, and T, respectively. The SPM tip is scanned at the speed of v. Here, the length of channel width is equal to the width of the groove. As shown in Fig. 5.13(a), the model provides a good fit to the experimental data with the length of 10 nm in the forward direction of SPM tip. However, the AFM image after scratching in the inset of Fig. 5.13(a) indicates the width of the groove is about 400 nm. Furthermore, in the experiment of up direction, although the groove width is estimated to be about 500 nm form the AFM image in the inset of Fig. 5.13(b), the experimental data are clearly fitted by the model assuming that the length is about 30 nm.

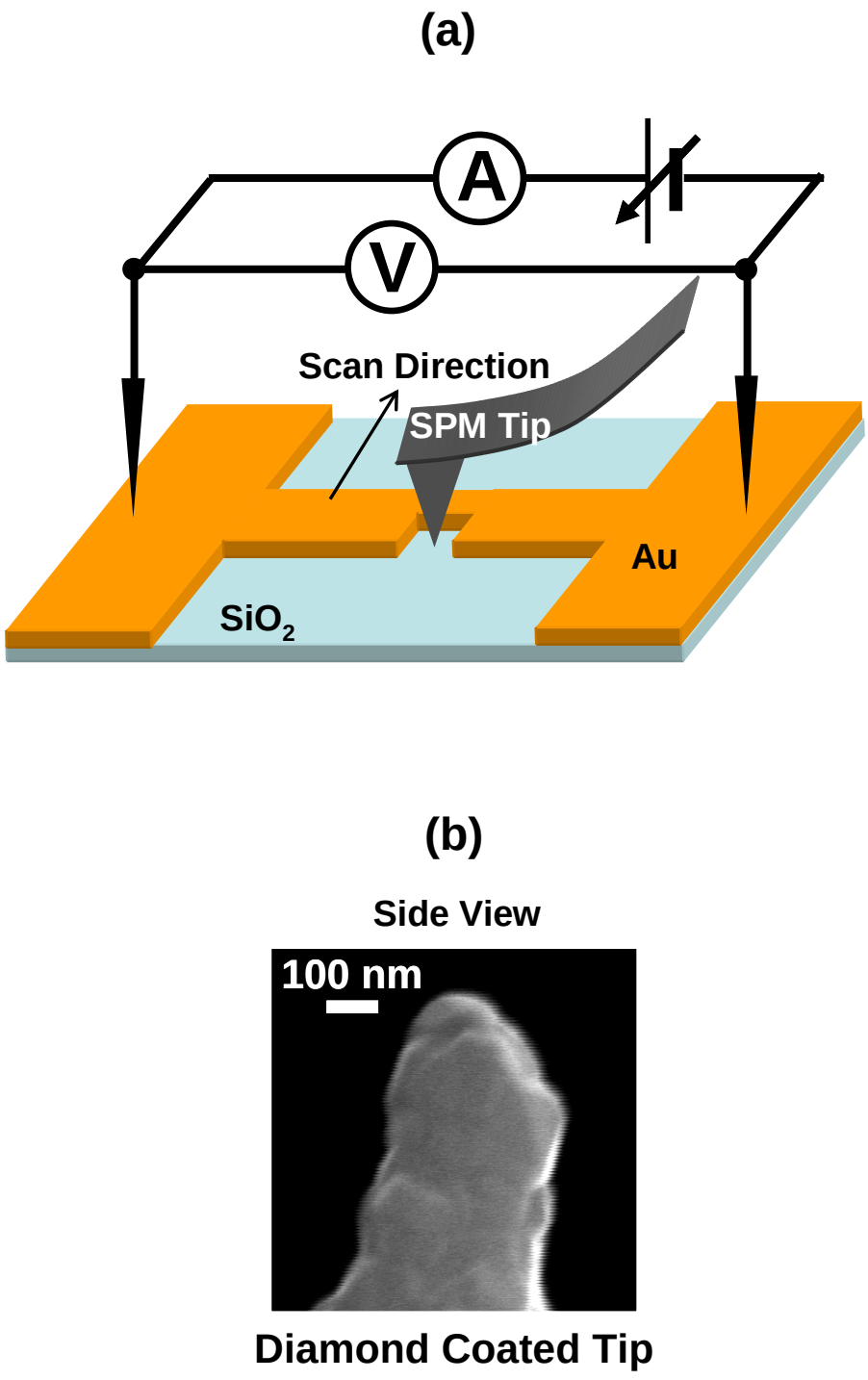


Fig. 5.7. (a) Schematic of SPM scratch lithography in Au. (b) SEM image of diamond coated SPM tip (side view).

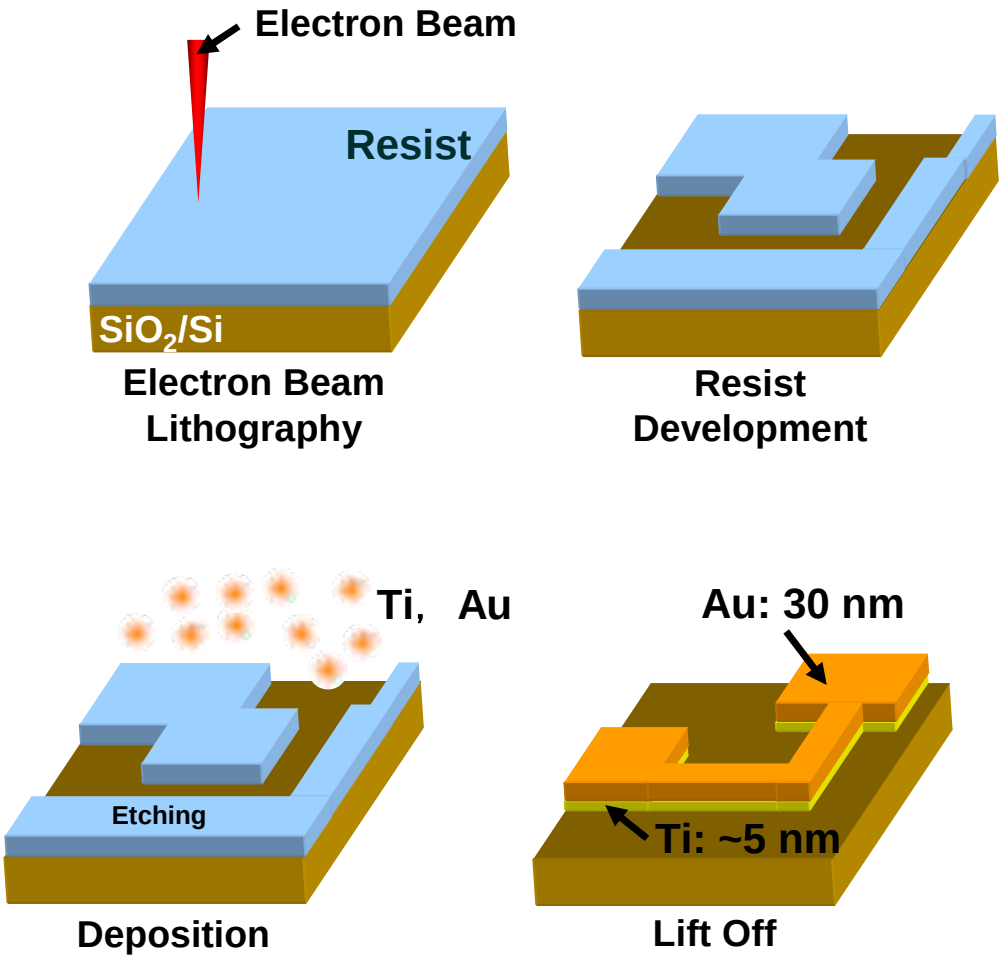


Fig. 5.8. The process flowchart of fabrication for planar-type Au wires.

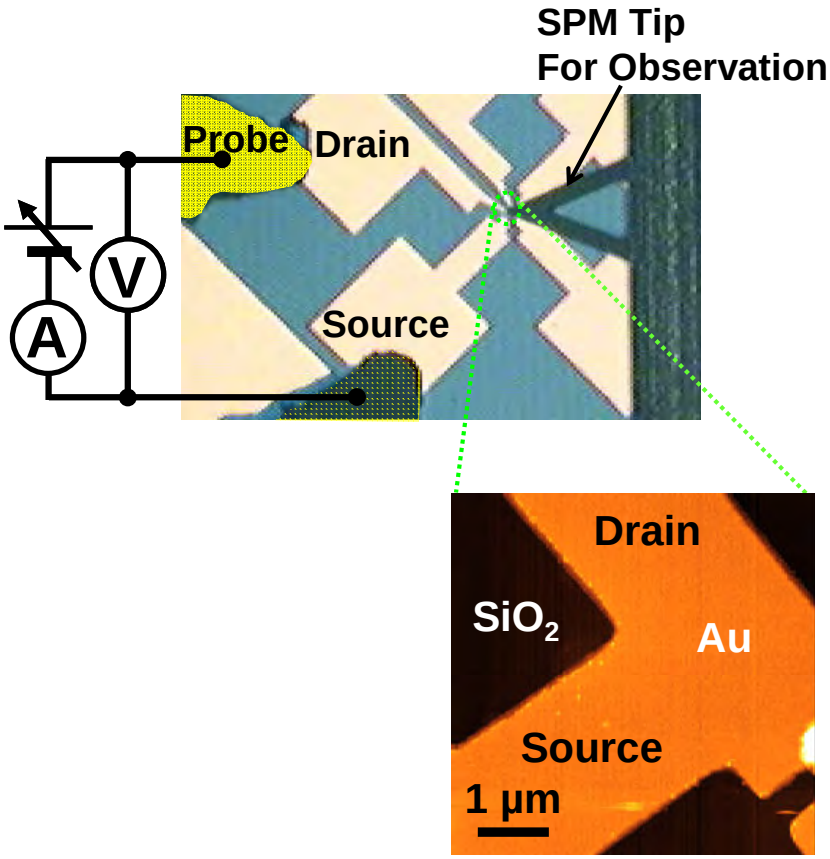


Fig. 5.9. Schematic of the experimental set-up in control of quantum states in Au and AFM image of Au wire.

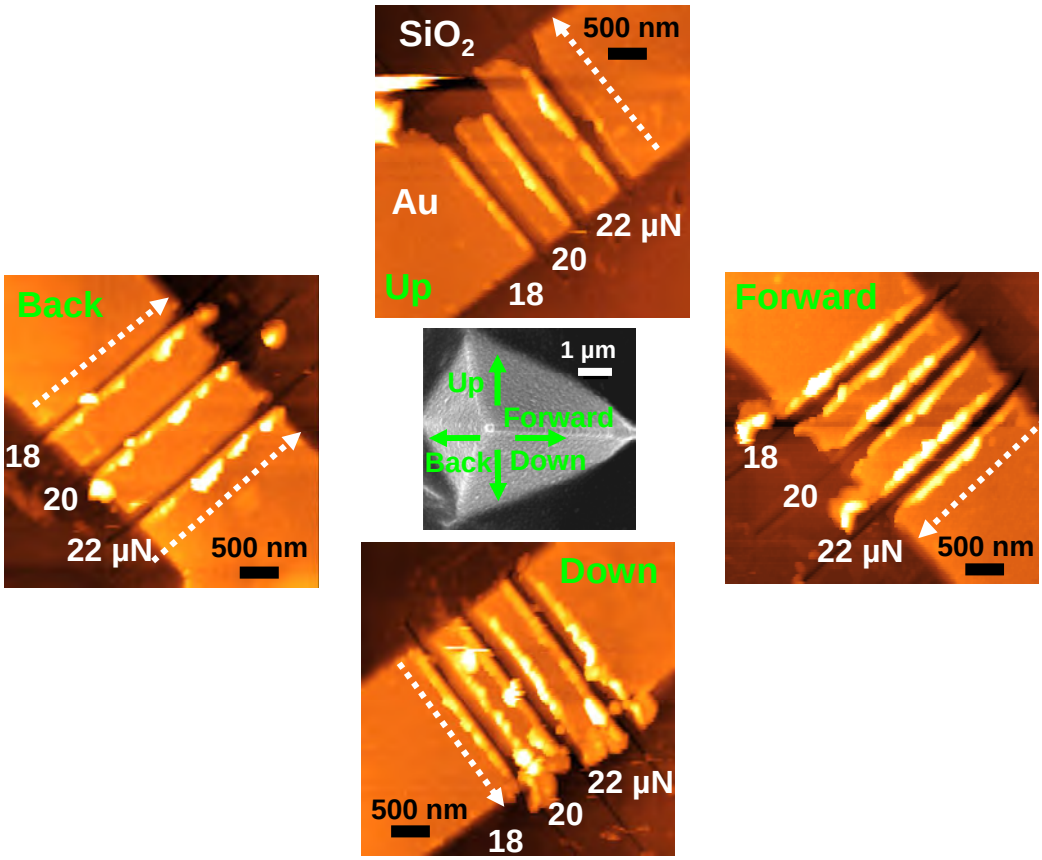


Fig. 5.10. AFM images of scratched Au wires. The applied force varies from 18 to 22 μN. Grooves were fabricated by one cycle in the various direction (Up, Down, Back, Forward).

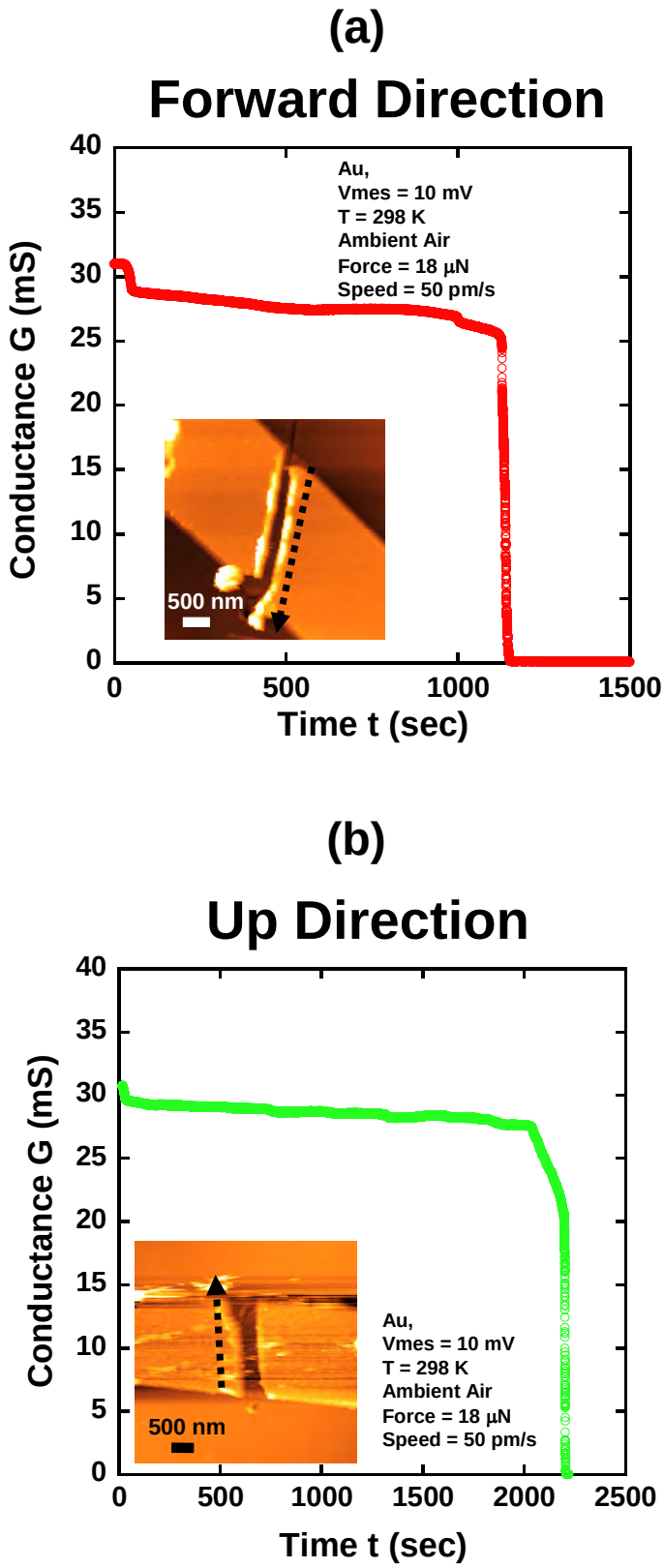


Fig. 5.11. (a) Conductance of Au wire as a function of time with scratching in the forward direction. (b) Conductance dependence of Au wire in process time for scratching in the up direction. In the experiments, the scanning speed of SPM tip and applied force were set at 50 pm/s and 18 μN, respectively.

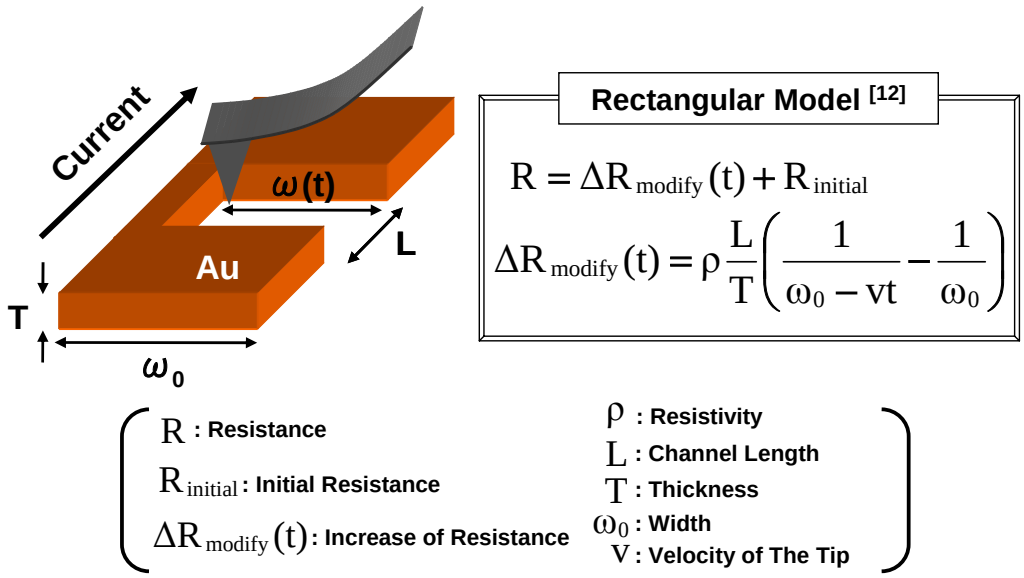


Fig. 5.12 The model of resistance modification in Au wires proposed by Snow et al.

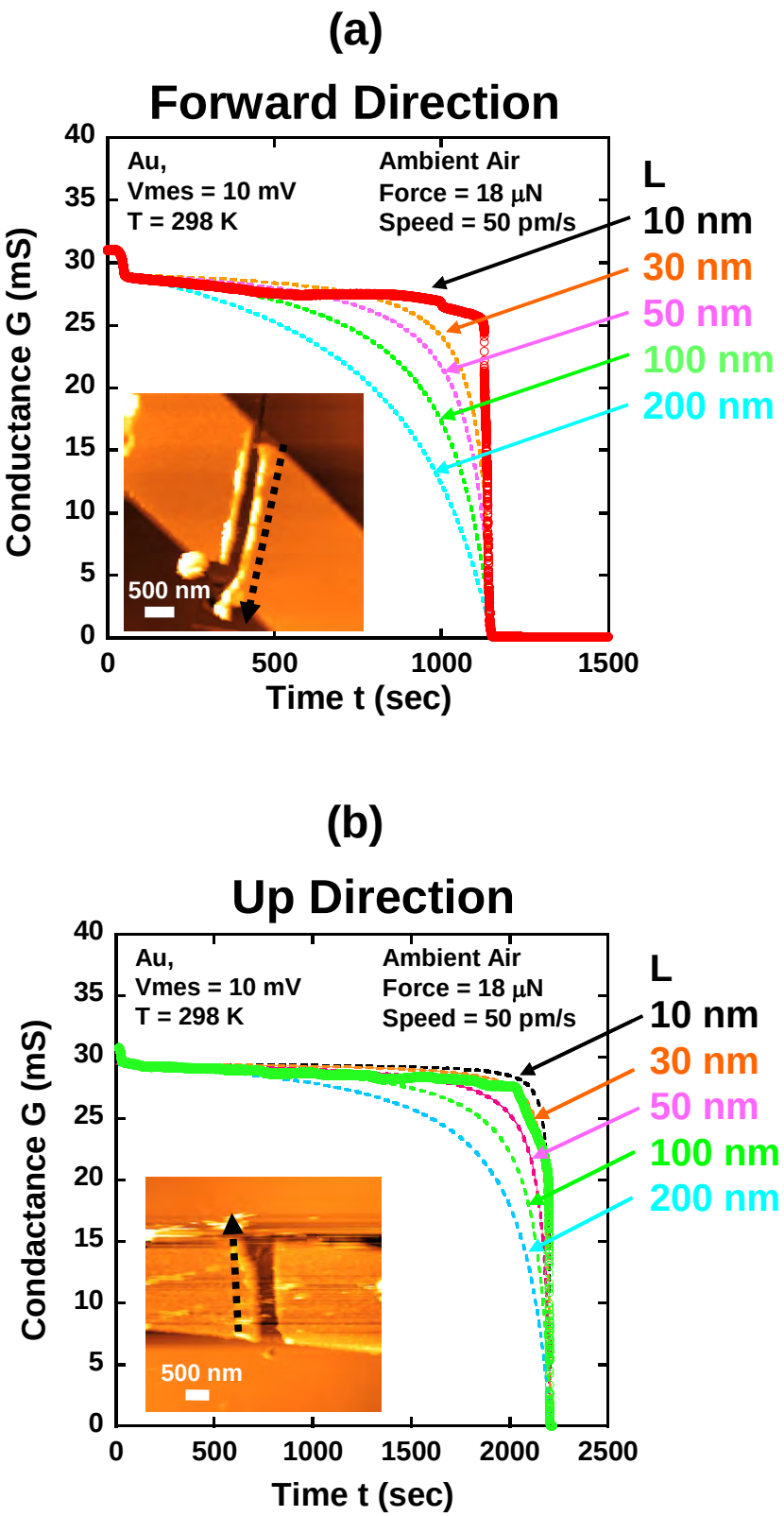


Fig. 5.13. (a) Conductance of Au wire as a function of time with scratching in the forward direction. (b) Conductance dependence of Au wire in process time for scratching in the up direction. In the experiments, the conductance of Au wire is fitted by Snow model.

In order to understand the relation between the Au channel size and the conductance of Au channel in detail, we propose the model of resistance modification in Au channel with a channel shape of trapezium as shown in Fig. 5.14. In this model, the increase of resistance in Au channel with respect to the time t during scratching nanolithography is described as follows,

$$\Delta R_{modify}(t) = \frac{\rho L}{Tb} \log\left(1 + \frac{b}{\omega_0 - vt}\right) \tag{5.5}$$

where b is the difference between the length of upper and lower base in trapezium. As shown in Fig. 5.15, the model with the length of 500 nm provides a good fits to the experimental data in forward and up direction of the SPM tip. These results are consistent with the width of the groove estimated from the AFM images in the inset of Figs. 5.15(a) and (b). Therefore, the model with channel shape of trapezium is suitable for the resistance modulation of Au channel with the sharp edges of single crystal diamond grains in SPM scratch nanolithography.

Trapezoidal Model

$$R = \Delta R_{modify}(t) + R_{initial}$$

$$\Delta R_{modify}(t) = \frac{\rho L}{Tb}\log\left(1 + \frac{b}{\omega_0 - vt}\right)$$

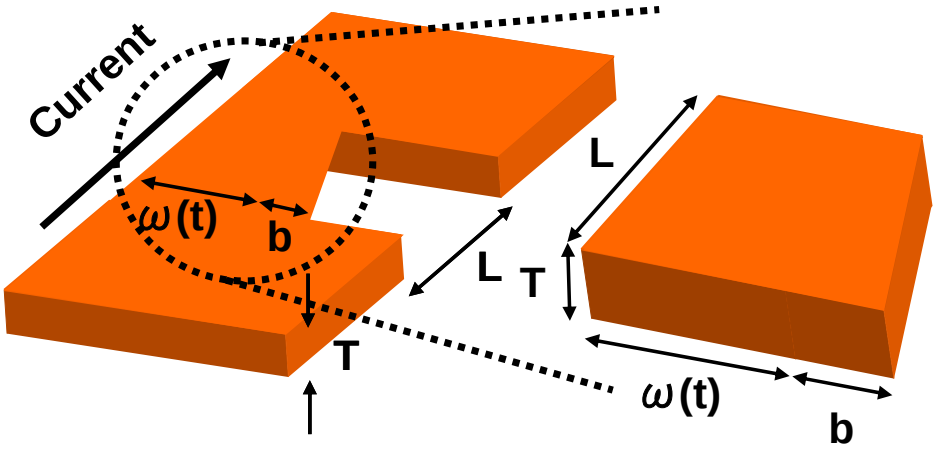


Fig. 5.14 The model of resistance modification in Au wires based on the channel shape (Trapezoidal).

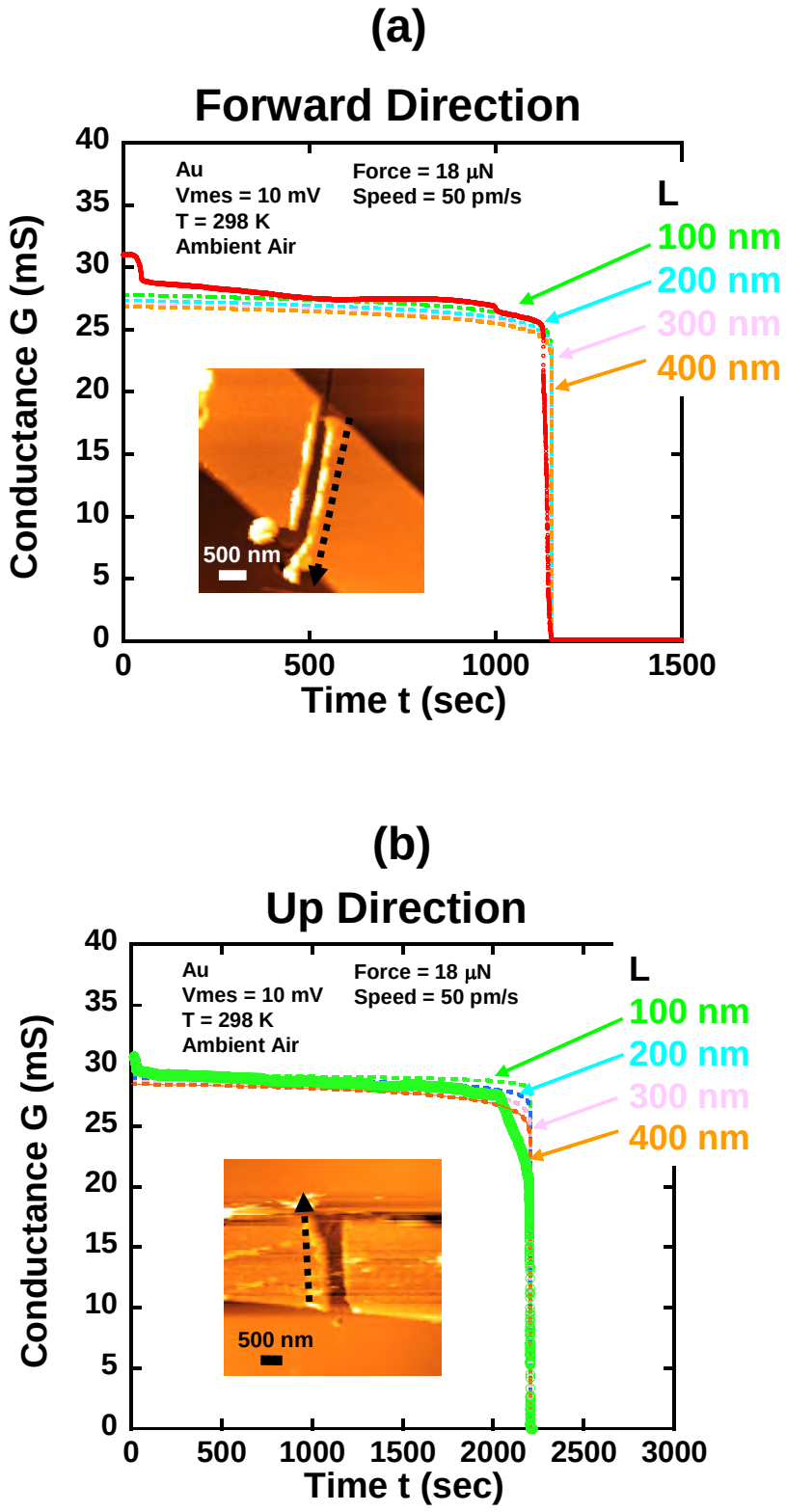


Fig. 5.15. (a) Conductance of Au wire as a function of time with scratching in the forward direction. (b) Conductance dependence of Au wire in process time for scratching in the up direction. In the figure, the conductance of Au wire is fitted by the model of resistance modification in Au wires based on the channel shape (Trapezoidal).

Figure 5.16(a) and (b) show the conductance below 12 G_0 ($G_0=2e^2/h$) in the forward and up direction. Here, the e is electron charge e and Planck constant h. As shown in the figures, conductance plateau was clearly observed below 12 G_0. Furthermore, the various scanning speed of SPM tip was applied to the sample in order to observe the QPC. As shown in Fig. 5.17, the conductance plateau is clearly observed when the scanning speed of SPM tip is set at 20 pm/s. Moreover, total time at each conductance plateau was plotted in Fig. 5.18. It is clearly indicated that the low scanning speed such as 20 pm/s is suitable for the fabrication of QPC in Au channel. These results suggested that the electrical properties of planar-type devices is easily controlled by SPM scratch nanolithography techniques.

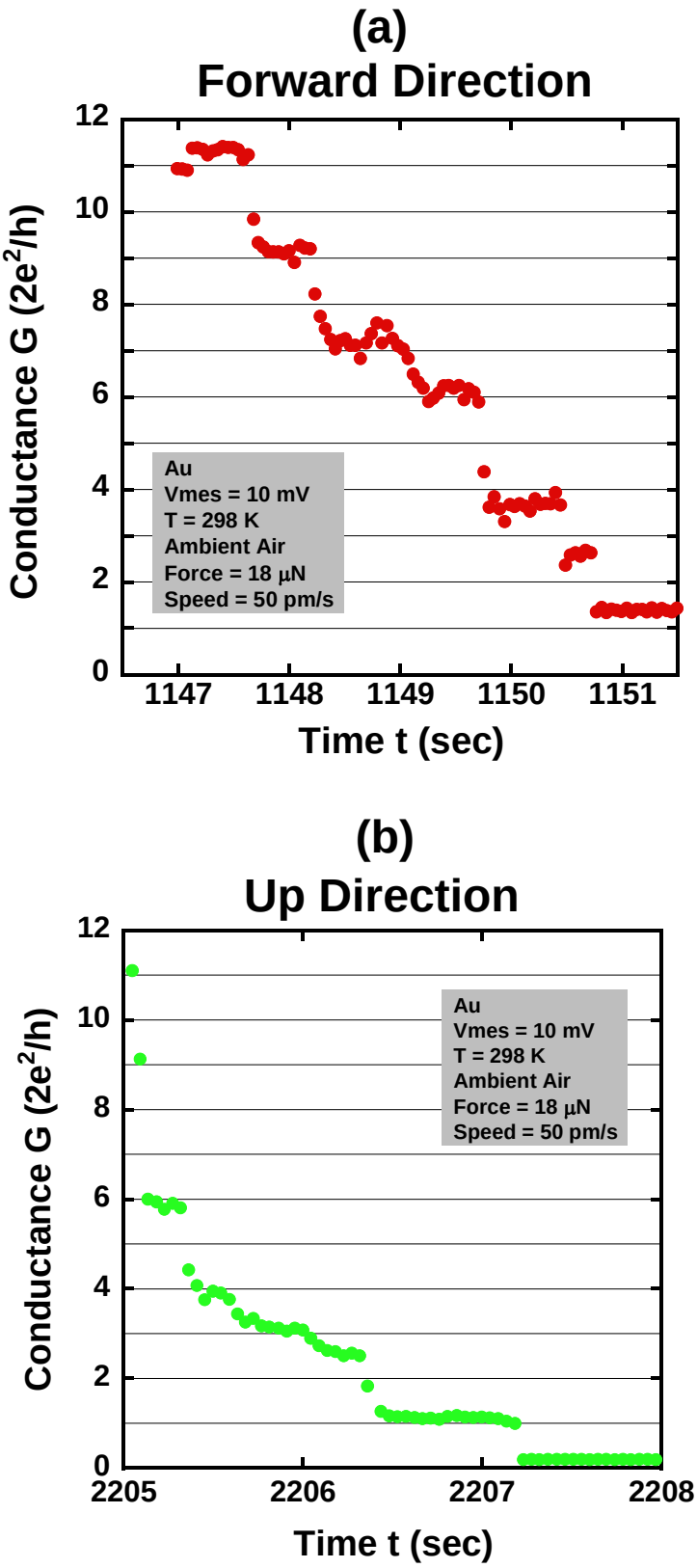


Fig. 5.16. (a) Conductance below 12 G_0 (=$2e^2/h$) of Au wire as a function of time with scratching in the forward direction. (b) Conductance below 12 G_0 (=$2e^2/h$) dependence of Au wire in process time for scratching in the up direction.

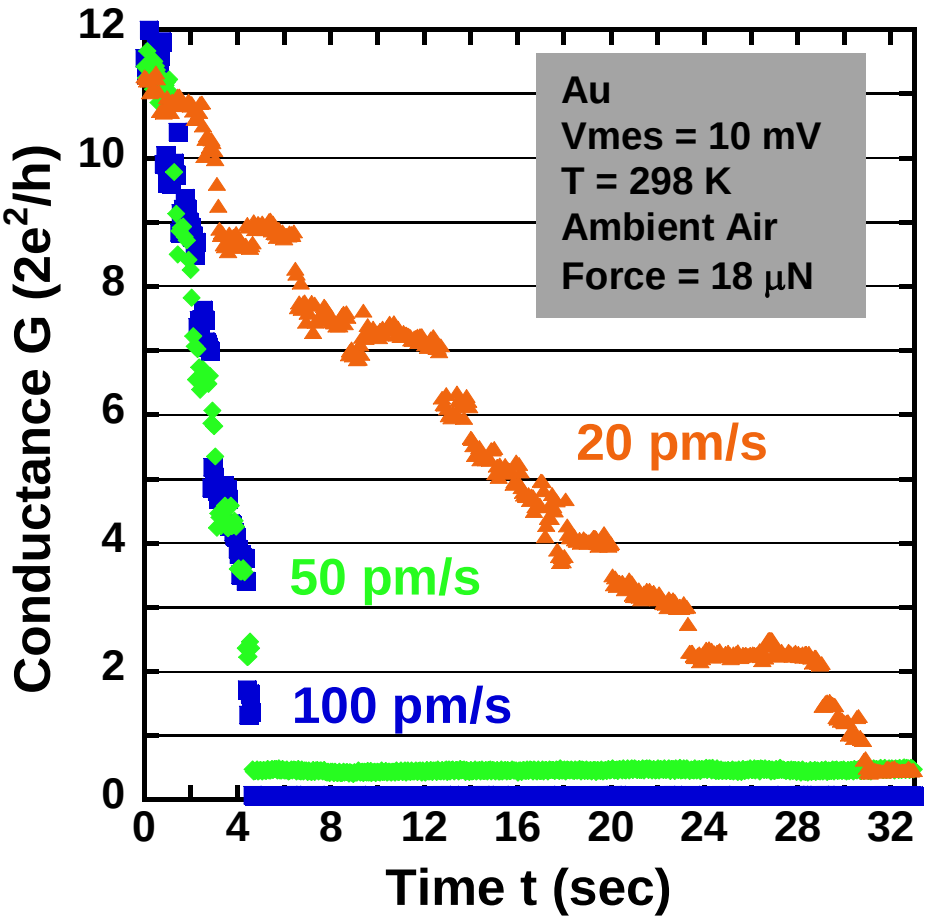


Fig. 5.17. Conductance below 12 G_0 (=$2e^2/h$) of Au wire as a function of time with scratching in the forward direction at various scanning speed of the SPM tip.

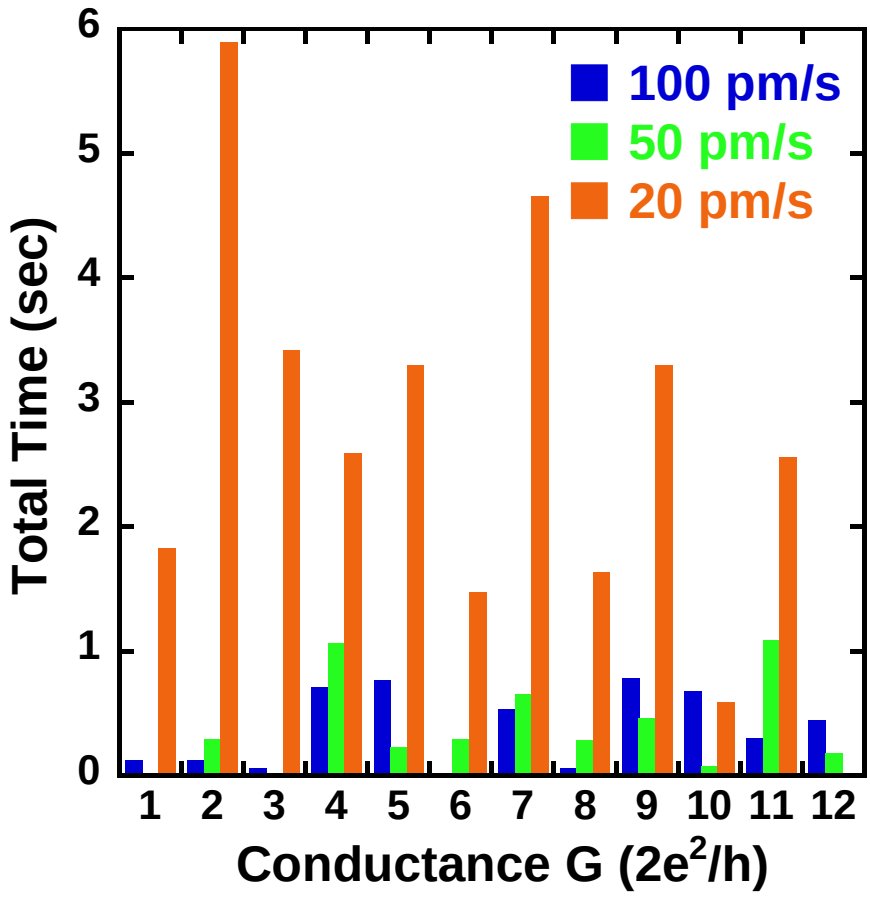


Fig. 5.18. Total time at each G_0 (=$2e^2/h$) versus conductance below 12 G_0 with scratching in the forward direction at various scanning speed of the SPM tip.

5.4 Magnetoresistive Effects in P-Type Silicon-On Insulator (SOI) Substrates

MR effect of P-Type silicon-on-insulator (SOI) substrate was investigated. The SOI substrate in this study consisted of 200 nm Si layer and 400 nm buried oxide (box) layer. Schematic illustrations of the SOI and direction of the applied magnetic field *B* are shown in Fig. 5.19(a) and (b), respectively. The carrier concentration and hole mobility are estimated by the Hall measurements, resulting in the values of 2.5×10^{16} cm^{-3} and 409 $cm^2/V \cdot s$, respectively. The current-voltage (I-V) characteristics were measured at 300 and 77 K. Here, MR is defined as $(R(B)/R(0) - 1) \times 100$ %, where $R(B)$ and $R(0)$ are the resistances at an applied magnetic field *B* and zero, respectively.

Figure 5.20(a) shows current and MR versus drain voltage characteristics of the P-type SOI substrate with the applied magnetic field *B* of 0 and 2.6 T at 300 K. The MR of SOI substrate gradually decrease from 10 to 0 % with the increase of the drain voltage. The MR dependences of the SOI substrate on the magnetic field were also measured in the Fig. 5.20(b). As shown in the figure, MR is enhanced with increase of the applied bias voltage from 0.6 to 1V. These MR characteristics are consistent with the result of IV and MR properties in Fig. 5.20(a).

Furthermore, MR of the SOI substrate are measured at the temperature of 77 K. The current is drastically suppressed at 77 K, and MR of 10 ~ 15 % is observed as shown in Fig. 5.21(a) and (b). These results show the MR effect also occurred in SOI substrate.

Here, the theoretical transverse MR is estimated at the electron mobility of 10^{15} and 10^{14} cm^{-3}. Transverse MR is one of the galvanomagnetic effects, in which a magnetic field perpendicular to an electric current gives rise to an electrical potential change in the direction of the current. From the Fig, 5.22, experimental MR is larger than the theoretical transverse

MR. These results indicate that the MR effects of SOI substrate are induced by physical phenomena such as space charge effects or impact ionization of carriers.

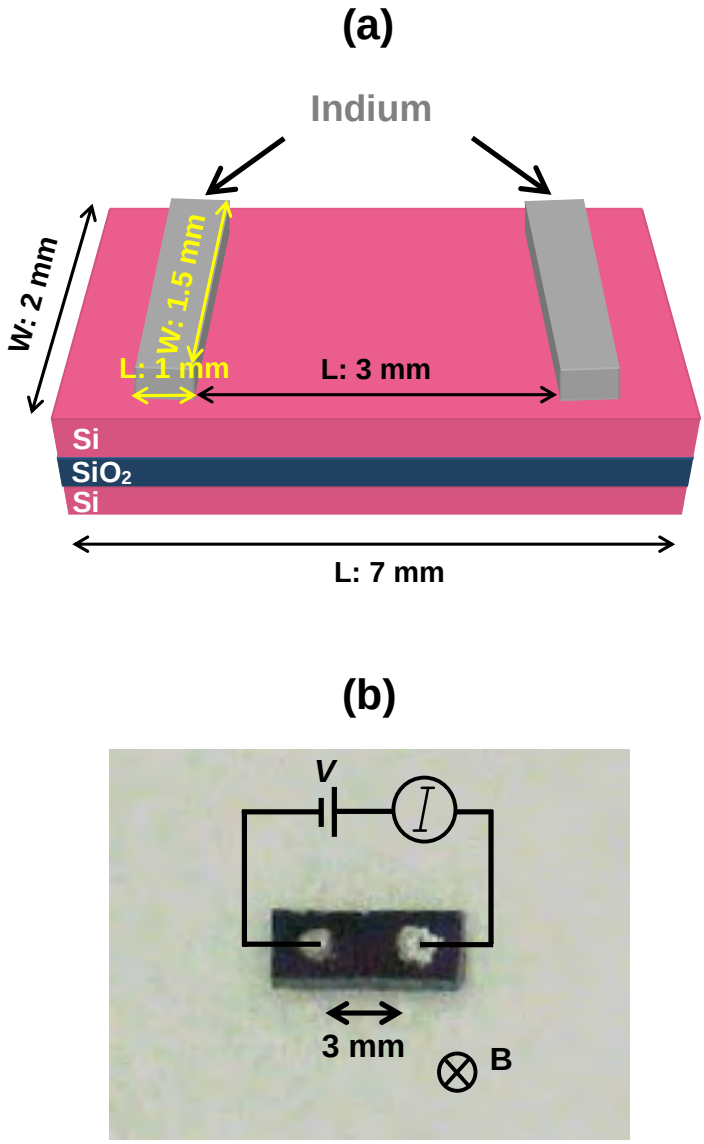


Fig. 5.19. (a) Schematic illustrations of the SOI and direction of the applied magnetic field *B* are shown in Fig. 6.1(a) and (b)

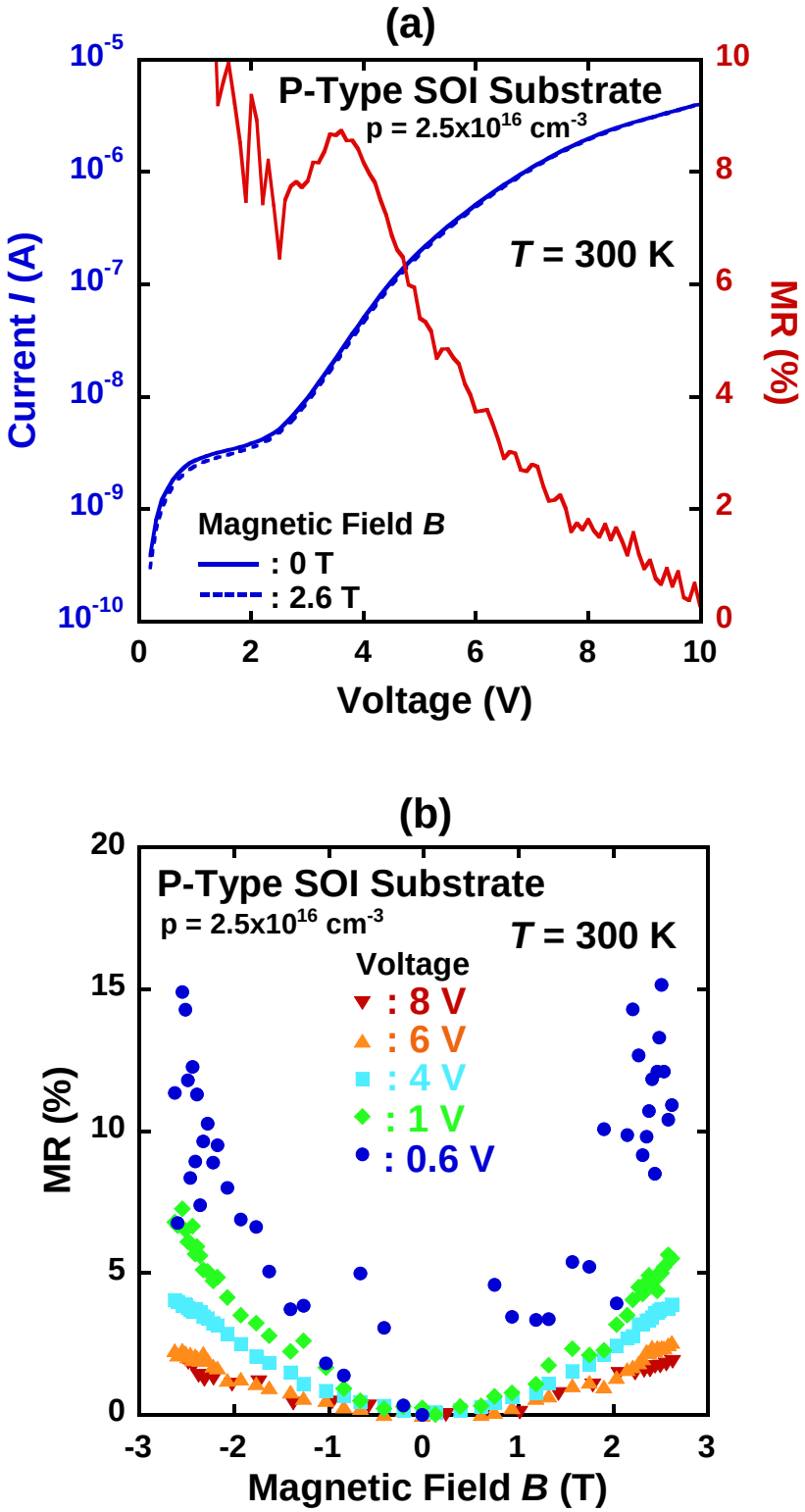


Fig. 5.20. (a) Current and MR versus drain voltage characteristics of the P-type SOI substrate with the applied magnetic field B of 0 and 2.6 T at 300 K. (b) MR dependences of the SOI substrate on the magnetic field.

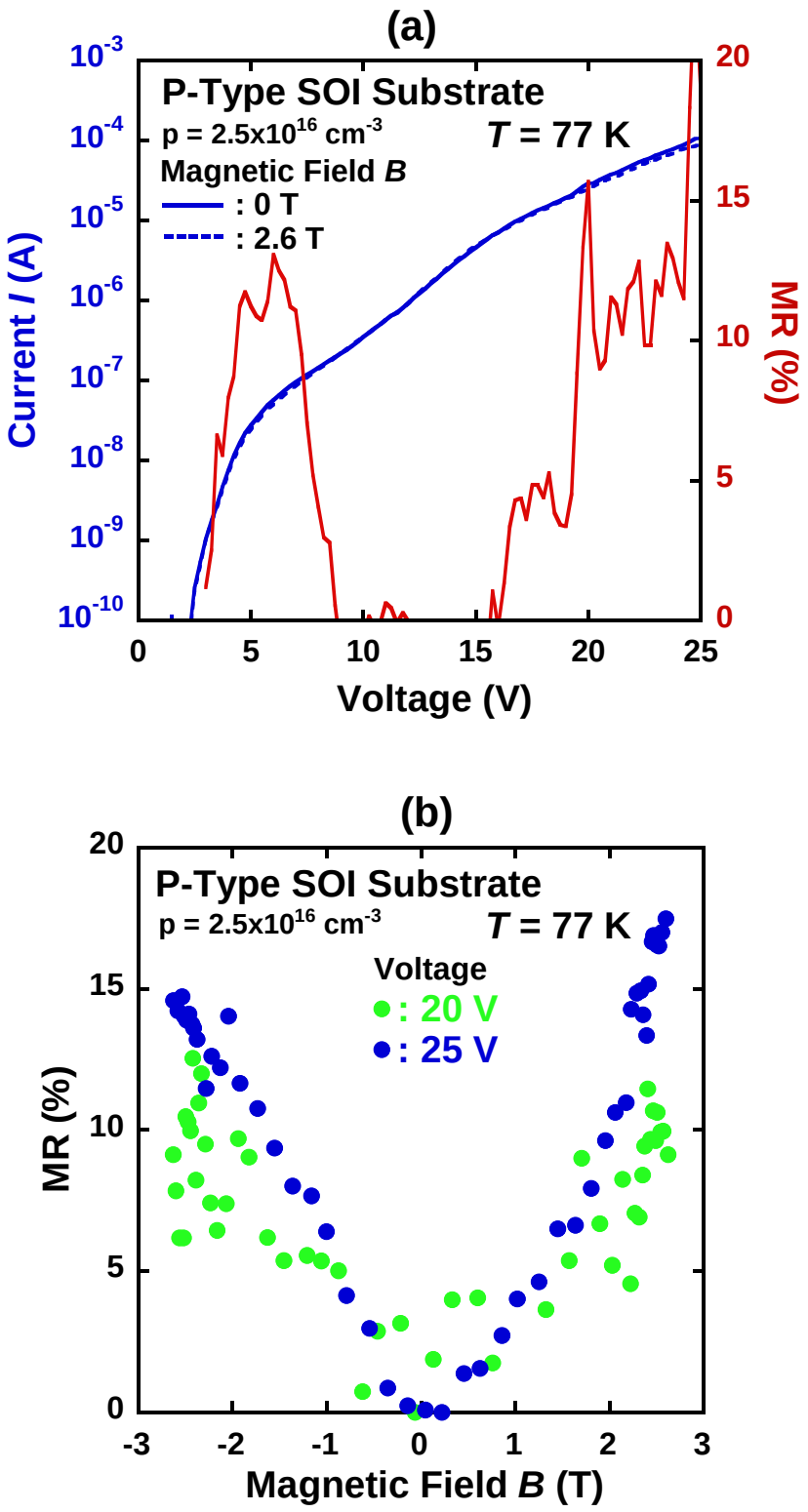


Fig. 5.21. (a) Current and MR versus drain voltage characteristics of the P-type SOI substrate with the applied magnetic field B of 0 and 2.6 T at 77 K. (b) MR dependences of the SOI substrate on the magnetic field.

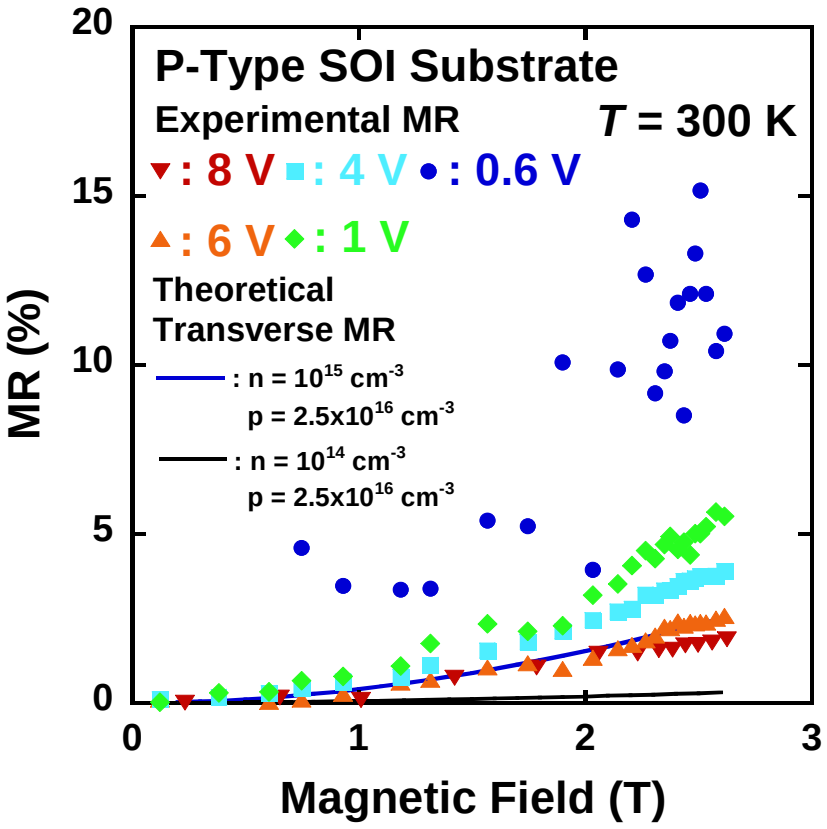


Fig. 5.22. MR dependences of the SOI substrate on the magnetic field as compared with transverse MR induced by galvanomagnetic effects.

5.5 Magnetoresistive Effects in Planar-Type Si Devices Using SPM Scratch Nanolithography

MR effect of P-Type silicon-on-insulator (SOI) substrate was confirmed to be ~ 15 % at room temperature. In this study, the MR of planar-type Si devices is measured at 300 K. As shown in Fig. 5.23, drain and gate contacts (Ni/Ti/Au = 20/10/70 nm) were defined by electron beam lithography and lift-off process. Figure 5.24 shows the optical images of fabricated planar-type Si devices and SEM image in the magnitude of Si channel. The width of Si channel is constricted to a few micrometers. In order to measure the MR of planar-Type Si devices, Al wires are bonded to the drain and gate contacts, as shown in Fig. 5.24. The magnetic field of 2.3 T is applied to perpendicular to the current flow.

Figure 5.25(a) shows drain current and MR versus drain voltage characteristics of the planar-type Si devices with the applied magnetic field B of 0 and 2.3 T at 300 K, when the gate voltage of 5 V is applied to the sample. The MR of planar-Type Si devices gradually decreases from 2 to 0 % with the increase of the drain voltage. The MR dependences of the planar-Type Si devices on the magnetic field were also measured in the Fig. 5.25(b). As shown in the figure, MR characteristics are consistent with the result of IV and MR properties in Fig. 5.25(a).

Figure 5.26(a) also shows drain current of the planar-type Si devices as a function of gate voltages at 300 K. Drain voltage of 1 V is applied to the sample. The MR dependences of the planar-type Si devices on the magnetic field at various gate voltages were measured. As shown in the Fig. 5.26(b), the MR of planar-type Si devices is observed at the value of 2 % and these MR characteristics are also consistent with the result of IV and MR properties in Fig. 5.26(a). These results indicate that planar-type Si devices also show the positive MR effects and MR is controlled by drain voltages. It is considered that the MR of semiconductor devices such as Si MOSFETs and JFETs strongly depend on the its carrier mobility, the

concentration of the carriers, and the geometry of the Si channel. If the SPM lithography is applied to the planar-type Si devices for narrowing the Si cannel, MR of planar-type Si devices may be enhanced.

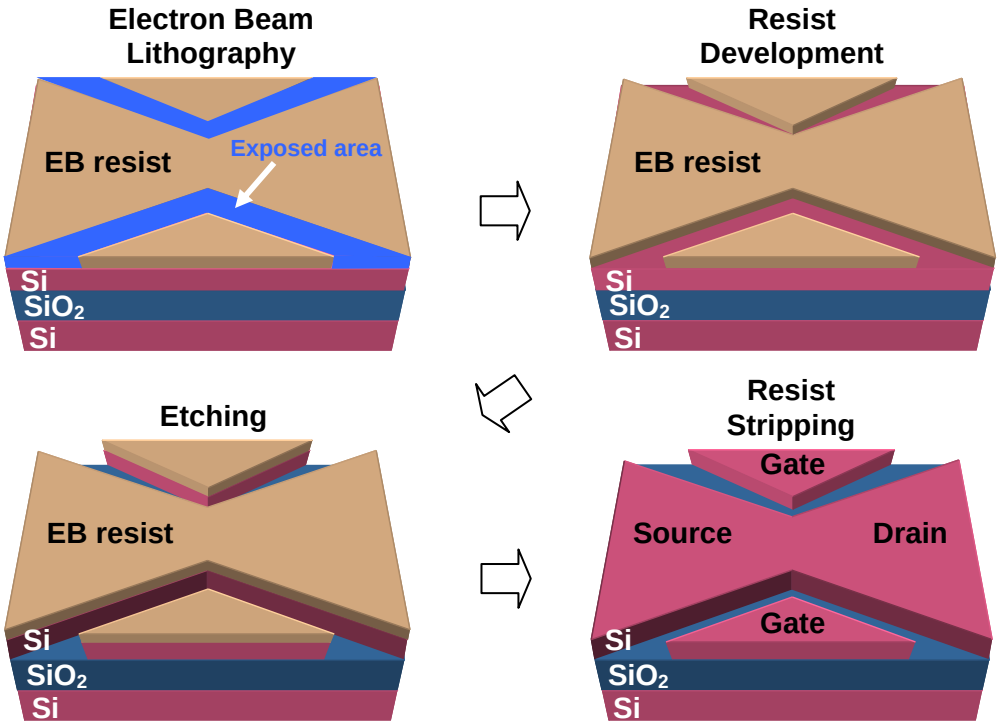


Fig. 5.23. The process flowchart of fabrication for planar-type Si devices.

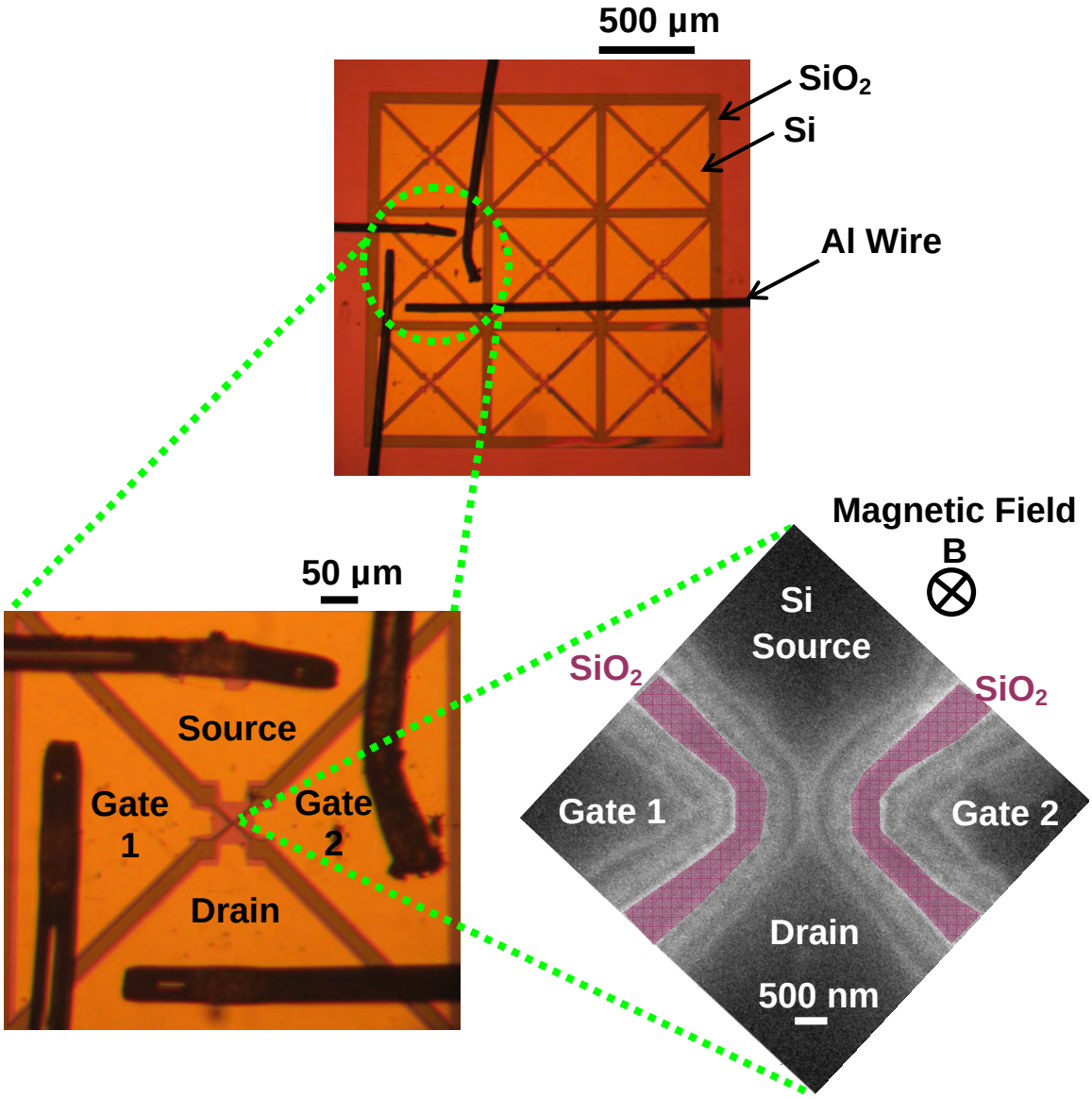


Fig. 5.24. Optical and SEM images of fabricated planar-type Si devices by EB lithography and wet etching process.

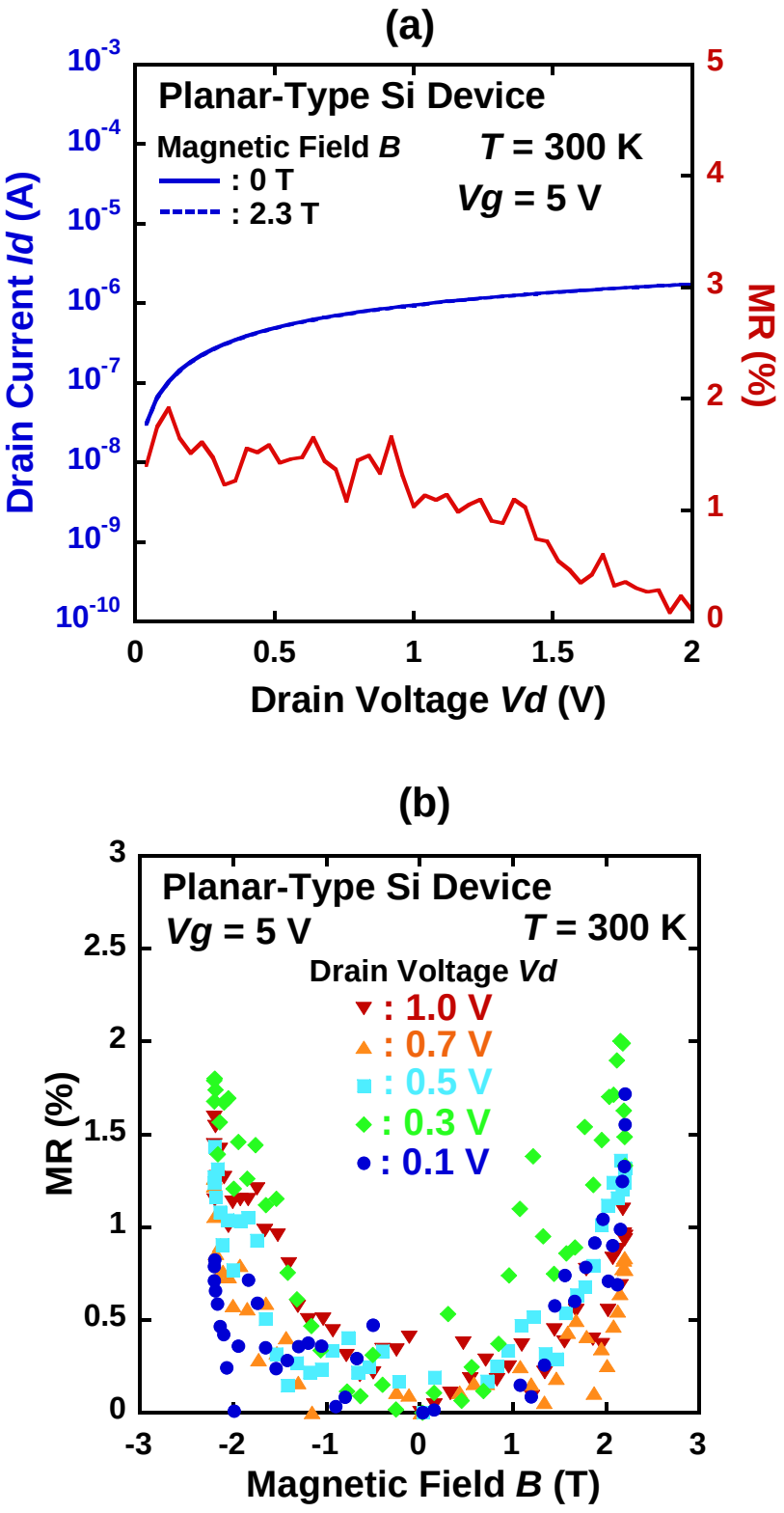


Fig. 5.25. (a) Drain current and MR versus drain voltage characteristics of the planar-type Si devices with the applied magnetic field B of 0 and 2.3 T at 300 K, when the gate voltage of 5 V is applied to the sample. (b) MR dependences of the planar-Type Si devices on the magnetic field with various drain voltages.

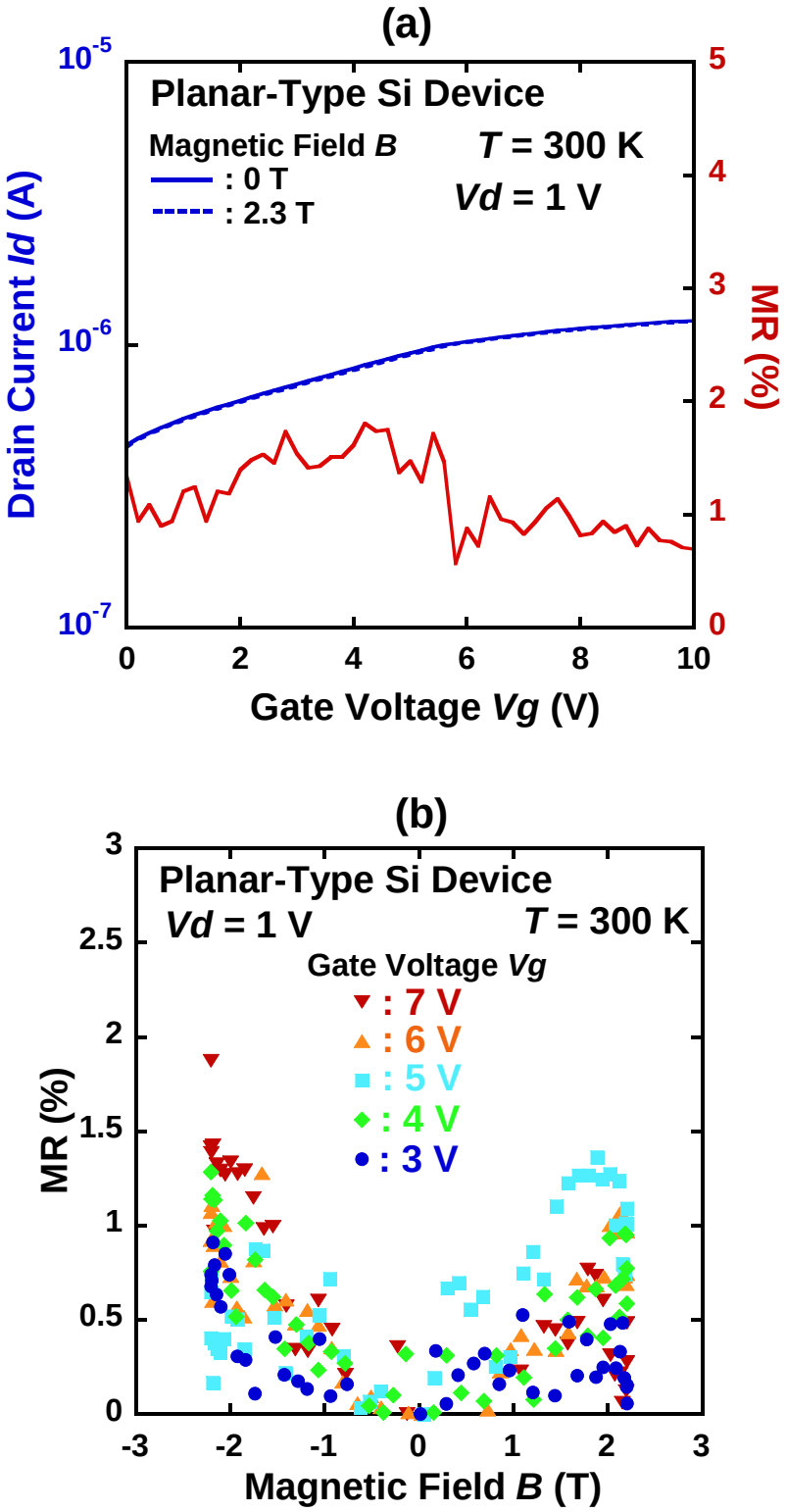


Fig. 5.26. (a) Drain current and MR versus gate voltage characteristics of the planar-type Si devices with the applied magnetic field *B* of 0 and 2.3 T at 300 K, when the drain voltage of 1 V is applied to the sample. (b) MR dependences of the planar-Type Si devices on the magnetic field with various gate voltages.

Figure 5.27 also shows the other sample of planar-type Si devices. Optical microscopy (OM), infrared (IR), and AFM image is described in the figure. All devices on the SOI substrate (carrier concentration of top layer = 4×10^{14} cm^{-3})are shown in Fig. 5.28 and consist of micrometer-scale Si channel. Here, the electrical properties and MR effect of planar-type Si devices are investigated.

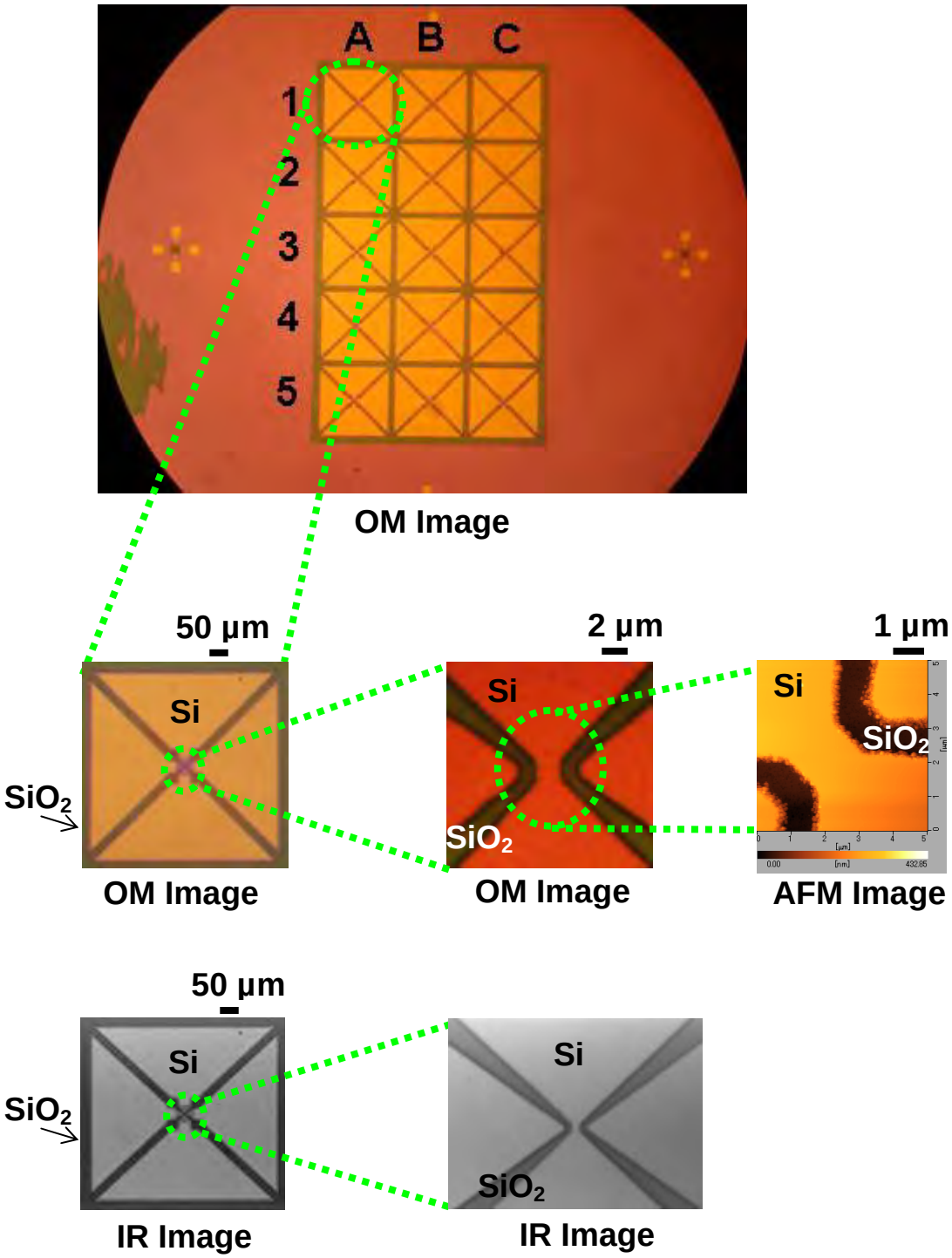


Fig. 5.27. Optical microscopy (OM), infrared (IR), and atomic micoscope (AFM) images of the planar-type Si devices.

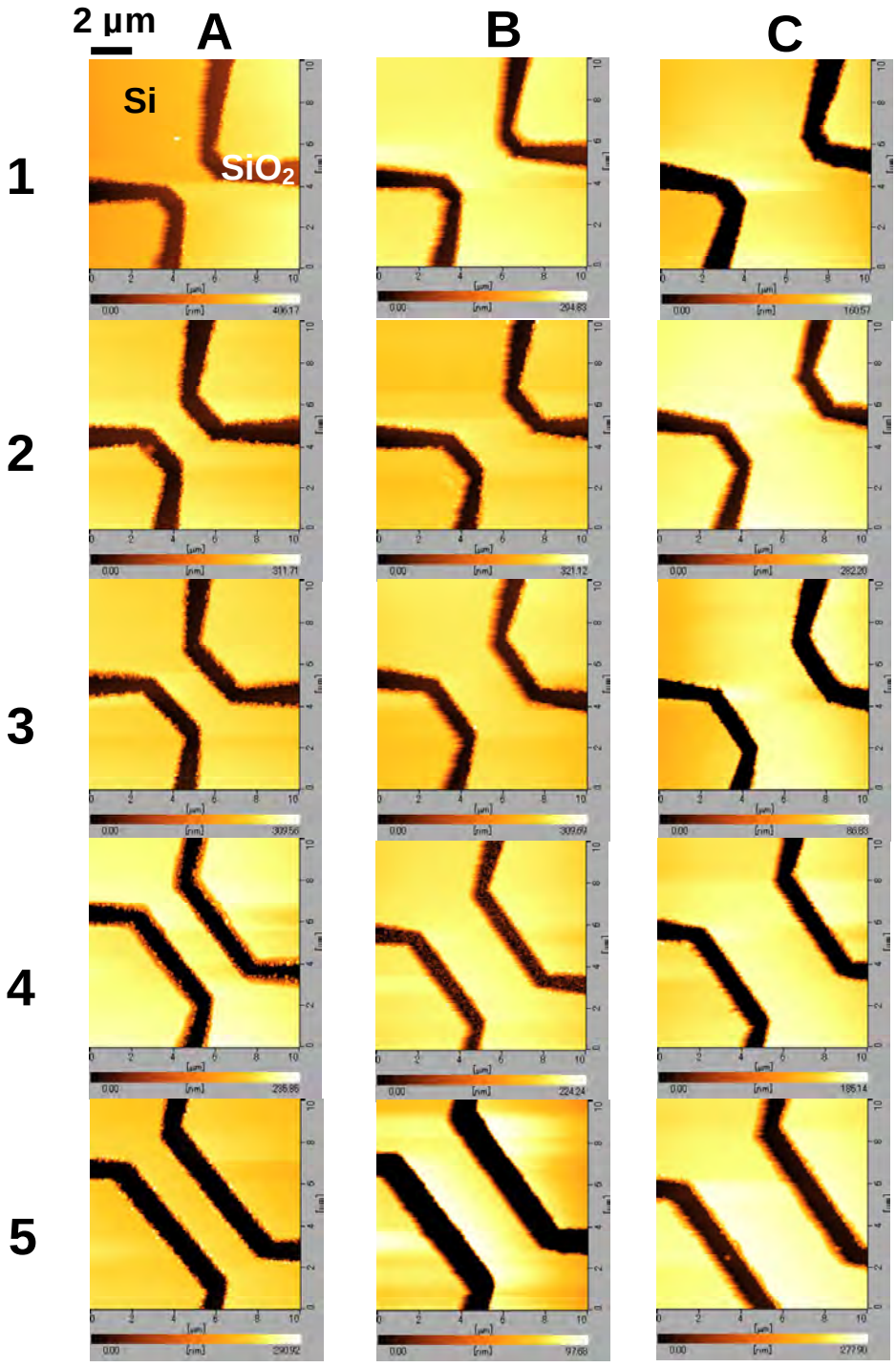


Fig. 5.28. ALL AFM images of the planar-type Si devices.

As shown in Fig. 5.29 (a) and (b), OM and AFM images clearly indicates that grooves are successfully formed in Si channel. The applied force is set to be 20 μN. Furthermore, drain current *Id* dependent of planar-type Si devices on the drain voltage *Vd* is described in Fig.5.30(a) and (b). Drain current is clearly suppressed after scratching lithography. Moreover, we also took the in-situ measurement of the Si channel during scratching. Furthermore, Fig. 5.31 shows that the effective electron mobility of *Vg* = 0 V estimated to be 200 $cm^2V^{-1}s^{-1}$ from the I-V properties in Fig. 5.30 with the fitting model of gradual channel approximation. The fitting model is expressed in the following foumula.

$$I_d = \frac{qN_D\mu W}{L}\left\{aV_d - \frac{2}{3}\left(\frac{2\varepsilon_s\varepsilon_0}{qN_D}\right)^{\frac{1}{2}}\left(V_d - V_g + V_d\right)^{\frac{3}{2}} + \frac{2}{3}\left(\frac{2\varepsilon_s\varepsilon_0}{qN_D}\right)^{\frac{1}{2}}\left(V_d - V_g\right)^{\frac{3}{2}}\right\} \qquad (5.6)$$

The carrier concentration is determined to be $N_D = 10^{17}$ cm^{-3}, which is estimated by Hall measurements. The thickness of the channel with the symbol of a is set to be 200 nm.

The current-voltage properties during scratching are shown in Fig. 5.32. This result clearly suggests that the conductance of Si channel is well controlled by scratch lithography. Furthermore, MR effects of planar-type Si devices were investigated. The current-voltage (I-V) characteristics were measured at 300K. Here, MR is defined as $(R(B)/R(0) - 1)\times 100$ %, where $R(B)$ and $R(0)$ are the resistances at an applied magnetic field B and zero, respectively. Figure 5.33 shows drain current *Id* and MR before and after scratching versus drain voltage *Vd* characteristics of the planar-type Si devices with the applied magnetic field *B* of 0 and 1.8 T at 300 K. The gate bias of 20 V is applied to the planar-type Si devices. From the figure, the drain currents after scratching are drastically suppressed. As shown in figure, the MR of the planar-type Si devices before and after scratching increases with the increase of drain voltages.

To clarify MR characteristics further, the MR before and after scratching dependences of the planar-type Si devices on the magnetic field were measured. Figures 5.34 show the MR

of the planar-type Si devices as a function of magnetic field at 300 K. The measurement at 300 K was carried out by applying a gate voltage of 0 V and a drain voltage of 0.5 V. As shown in the figure, the 300 K MR shows a continuous increase, reaching about 0.6 % at the magnetic field of 1.8 T.

If the MR induced by the geometrical effect occurs and dominates in the planar-type Si devices, the MR of the planar-type Si devices may be expressed as $MR_{geo} = \mu^2 B^2$ x 100 %, which is described in Chapter. 2. In this device, the gate length *L* and width *W* is estimated to be 1.3 and 2 μm form the AFM image in Fig. 5.29. Furthermore, the effective electron mobility is estimated to be 200 $cm^2V^{-1}s^{-1}$ from the I-V properties in Fig. 5.30. Therefore, MR induced by the geometrical effect (MR_{geo}) at the magnetic field of 1.8 T is assumed to be MR_{geo} = 0.1 %. However, the MR observed in the experiments (MR_{exp}) is MR_{exp} = 0.5 %, which is about 5 times larger than that of the MR induced by the geometrical effect. Recently, it has been previously discussed by Ciccarelli *et al.* that MR of the Si MOSFET below the threshold voltage at 4.2 K has to be associated with space charge transport regime [12]. Therefore, it is suggested that the MR of the planar-type Si devices may arise from physical MR effects, such as the impact ionization of carriers [13, 14] and space charge effect [15-17], with the combination of the geometrical MR effect.

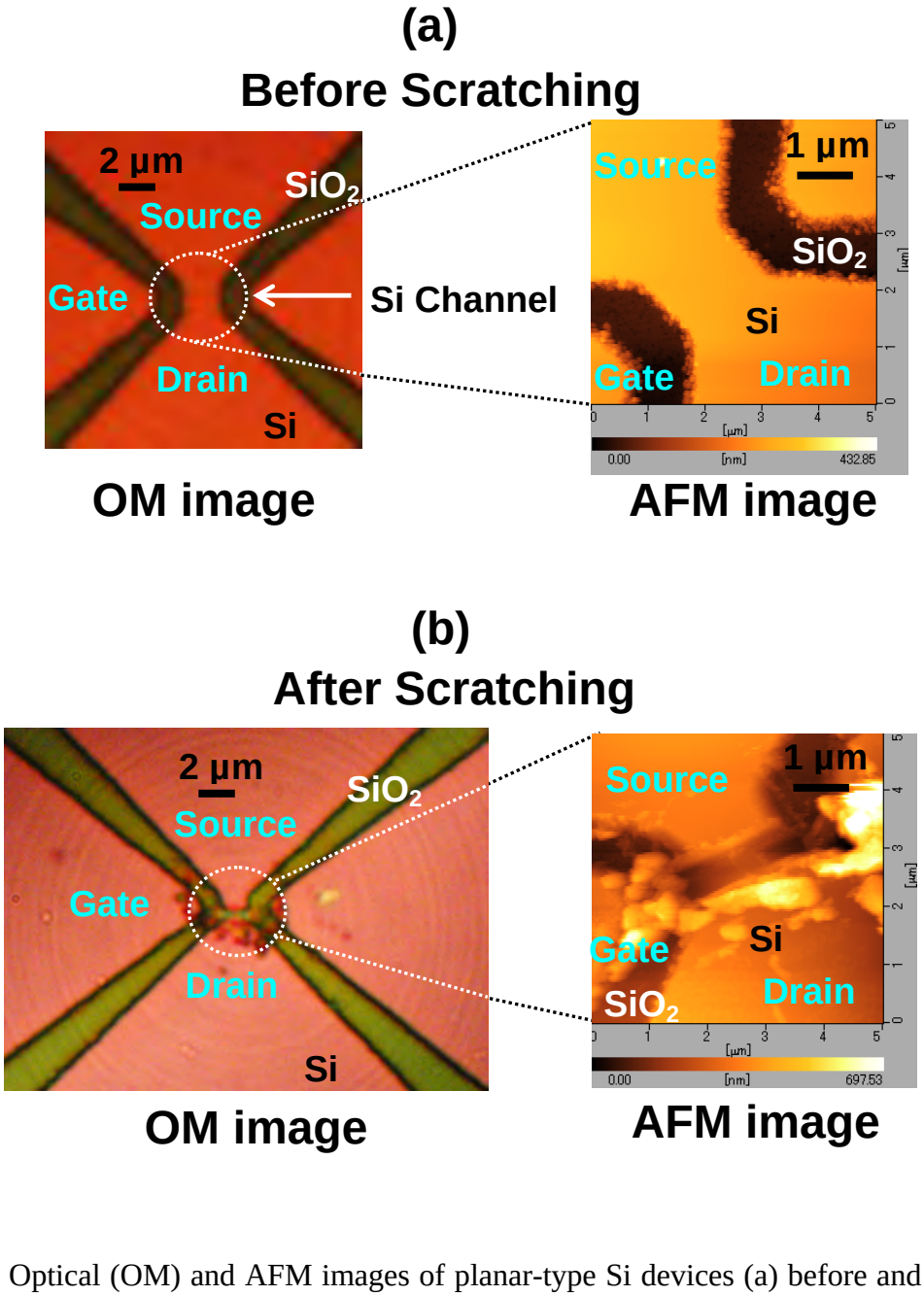


Fig. 5.29. Optical (OM) and AFM images of planar-type Si devices (a) before and (b) after scratching. (W/L = 1.5)

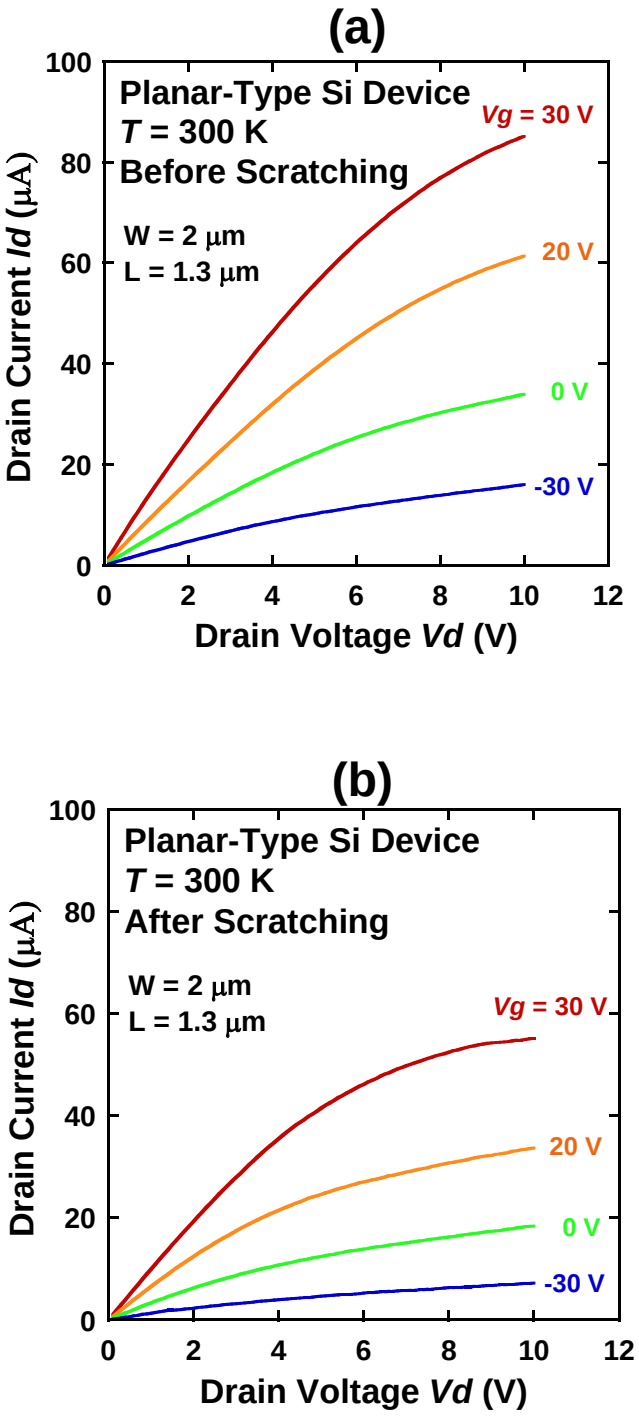


Fig. 5.30. (a) Drain current *Id* of planar-type Si device with various gate voltages as a function of drain voltage *Vd* (a) before and (b) after scratching. (W/L = 1.5)

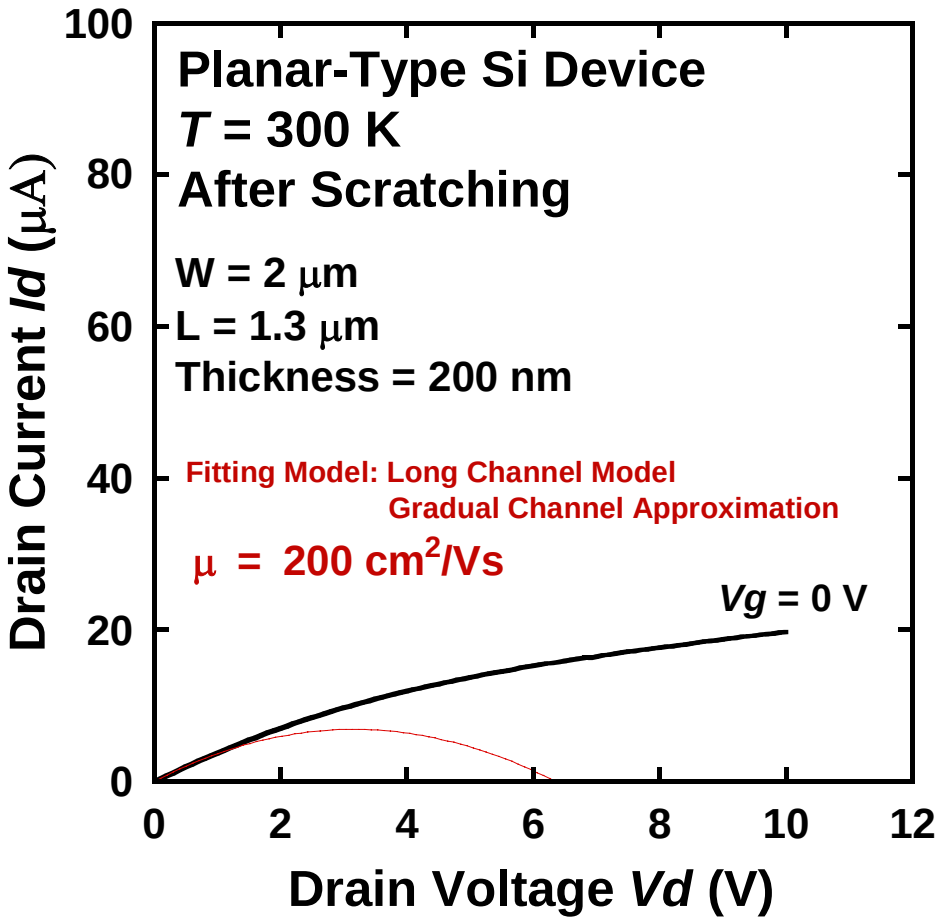


Fig. 5.31. Drain current *Id* of planar-type Si device with gate voltages of 0 V as a function of drain voltage *Vd*. (W/L = 1.5) The model with gradual channel approximation at μ = 200 $cm^2/V \cdot s$ is fitted to experimental data.

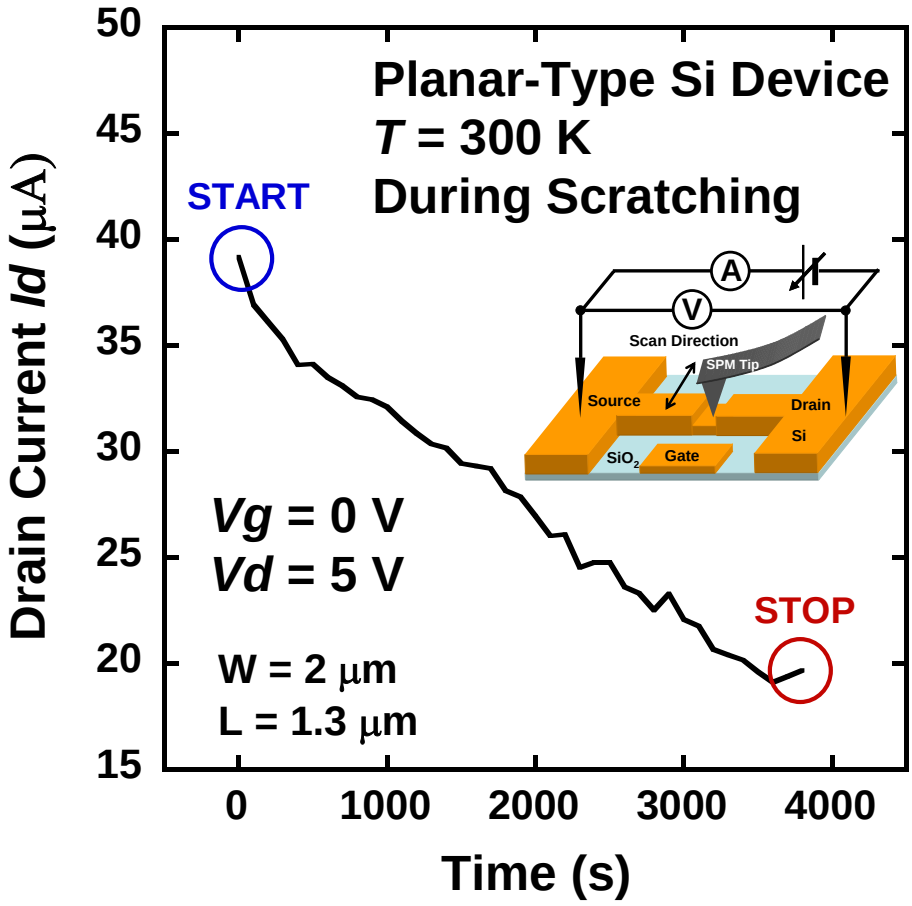


Fig. 5.32. Drain current *Id* of planar-type Si device with *Vg* = 0 V, *Vd* = 5 V as a function of time during scratching process. (W/L = 1.5)

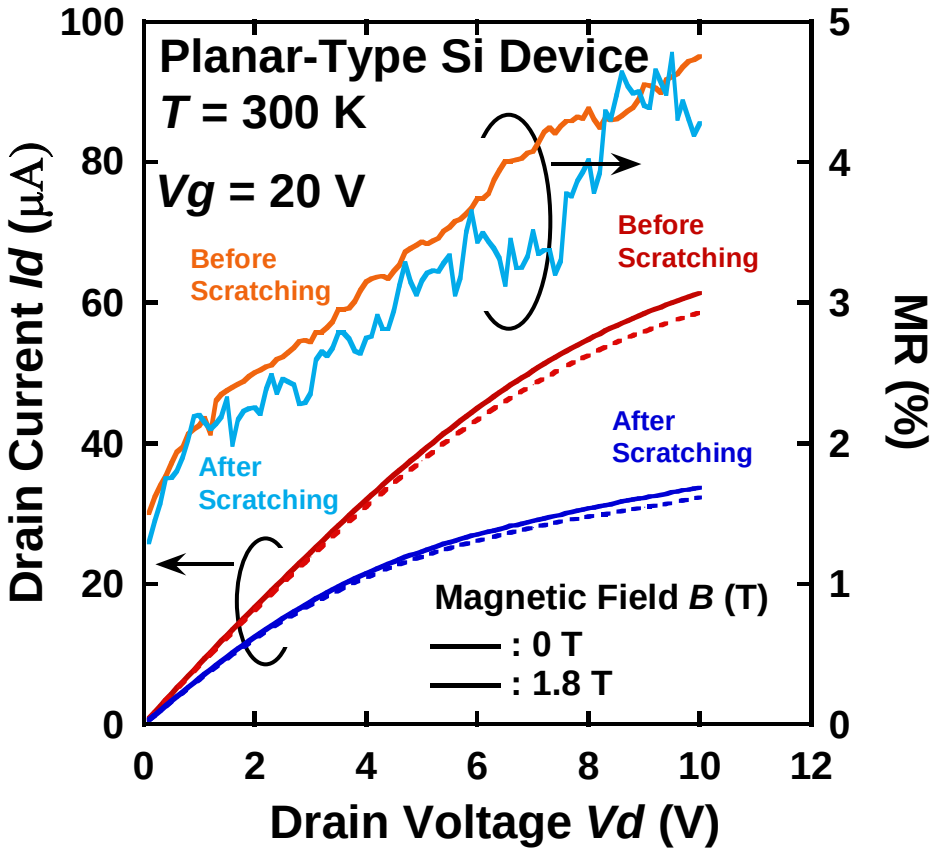


Fig. 5.33. Drain current *Id* and MRof planar-type Si device with *Vg* = 20 V as a function of drain voltage *Vd*. Magnetic field of 1.8 T is applied to the perpendicular to drain current *Id*. (W/L = 1.5)

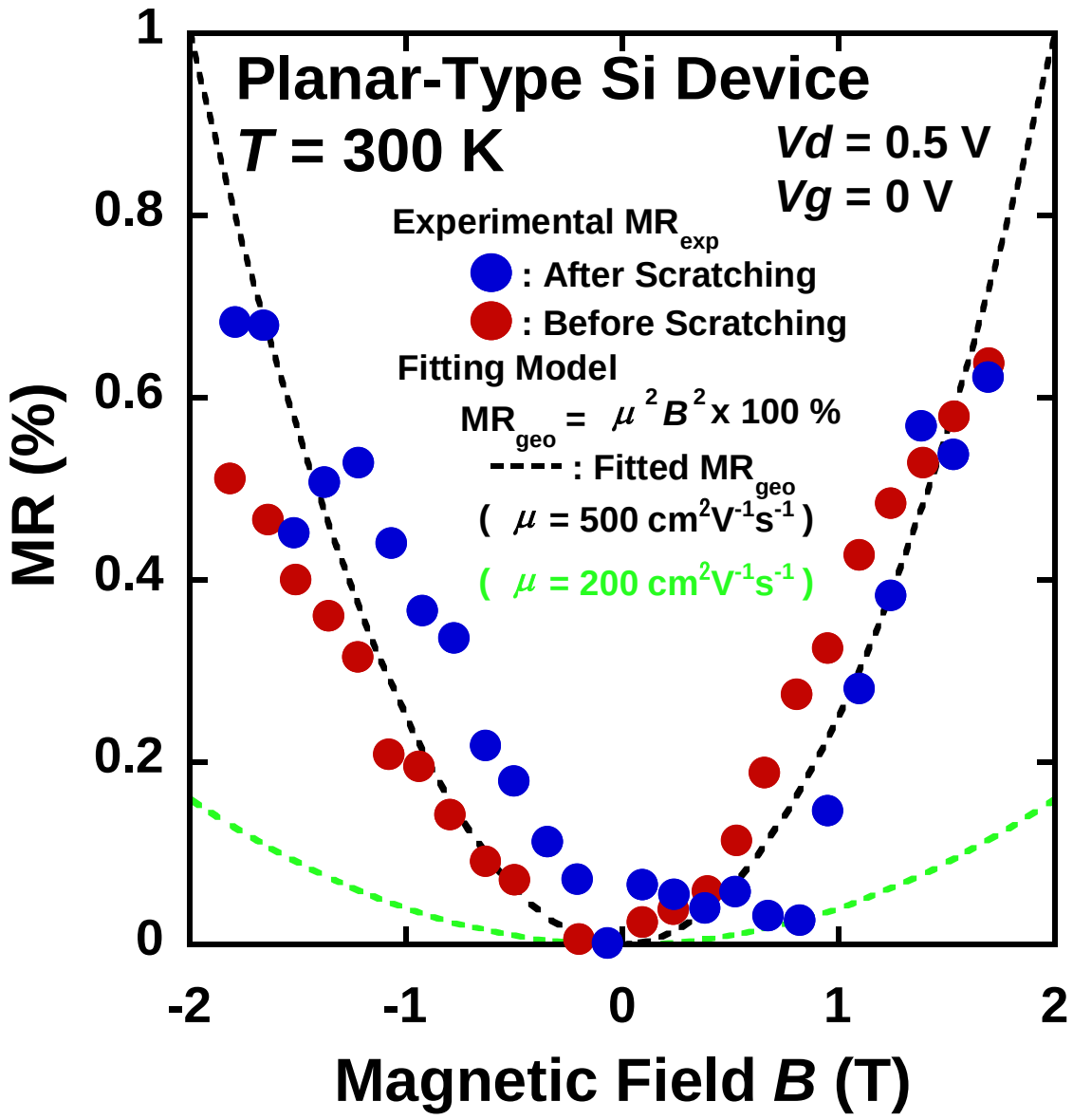


Fig. 5.34. MR of planar-Type Si Device as a function of magnetic field *B* at 300 K. (W/L = 1.5)

As shown in Fig. 5.35 (a) and (b), OM and AFM images clearly indicates that grooves are successfully formed in Si channel. The applied force is set to be 20 μN. Furthermore, drain current *Id* dependent of planar-type Si devices on the drain voltage *Vd* is described in Fig.5.36(a) and (b). Drain current is clearly suppressed after scratching lithography. Moreover, we also took the in-situ measurement of the Si channel during scratching. Furthermore, Fig. 5.37 shows that the effective electron mobility of Vg = 0 V estimated to be 200 $cm^2V^{-1}s^{-1}$ from the I-V properties in Fig. 5.36 with the fitting model of gradual channel approximation. The carrier concentration is determined to be 10^{17} cm^{-3}, which is estimated by Hall measurements.

To clarify MR characteristics further, the MR before and after scratching dependences of the planar-type Si devices on the magnetic field were measured. Figures 5.38 show the MR of the planar-type Si devices as a function of magnetic field at 300 K. The measurement at 300 K was carried out by applying a gate voltage of 0 V and a drain voltage of 0.5 V. As shown in the figure, the 300 K MR shows a continuous increase, reaching about 0.6 % at the magnetic field of 1.8 T.

If the MR induced by the geometrical effect occurs and dominates in the planar-type Si devices, the MR of the planar-type Si devices may be expressed as $MR_{geo} = \mu^2B^2$ x 100 %, which is described in Chapter. 2. In this device, the gate length L and width W is estimated to be 7.7 and 2.8 μm form the AFM image in Fig. 5.35. Furthermore, the effective electron mobility is estimated to be 200 $cm^2V^{-1}s^{-1}$ from the I-V properties in Fig. 5.36. Therefore, MR induced by the geometrical effect (MR_{geo}) at the magnetic field of 1.8 T is assumed to be MR_{geo} = 0.1 %. However, the MR observed in the experiments (MR_{exp}) is MR_{exp} = 0.5 %, which is about 5 times larger than that of the MR induced by the geometrical effect. Recently, it has been previously discussed by Ciccarelli *et al.* that MR of the Si MOSFET below the threshold voltage at 4.2 K has to be associated with space charge transport regime [12].

Therefore, it is suggested that the MR of the planar-type Si devices may arise from physical MR effects, such as the impact ionization of carriers [13, 14] and space charge effect [15-17], with the combination of the geometrical MR effect.

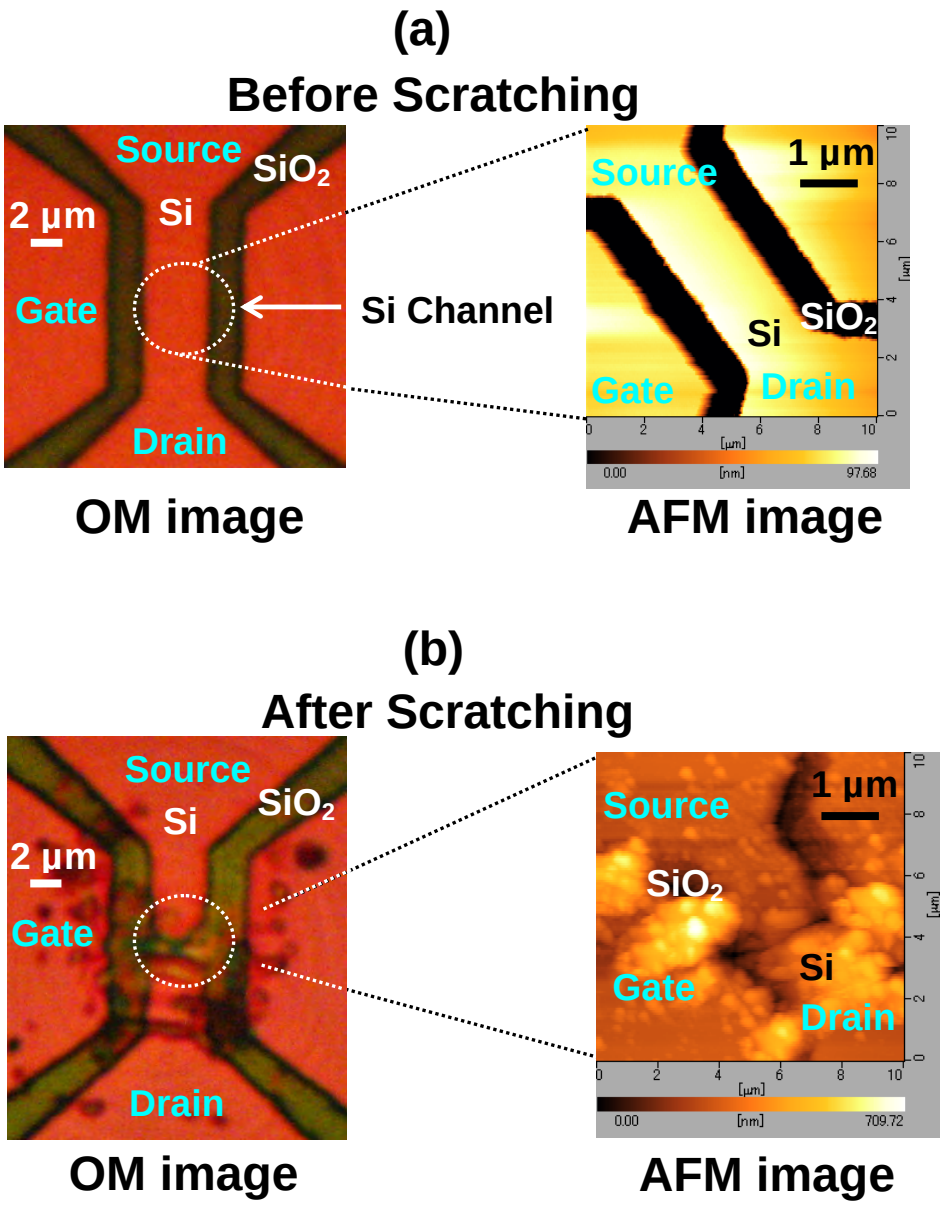


Fig. 5.35. Optical (OM) and AFM images of planar-type Si devices (a) before and (b) after scratching. (W/L = 0.4)

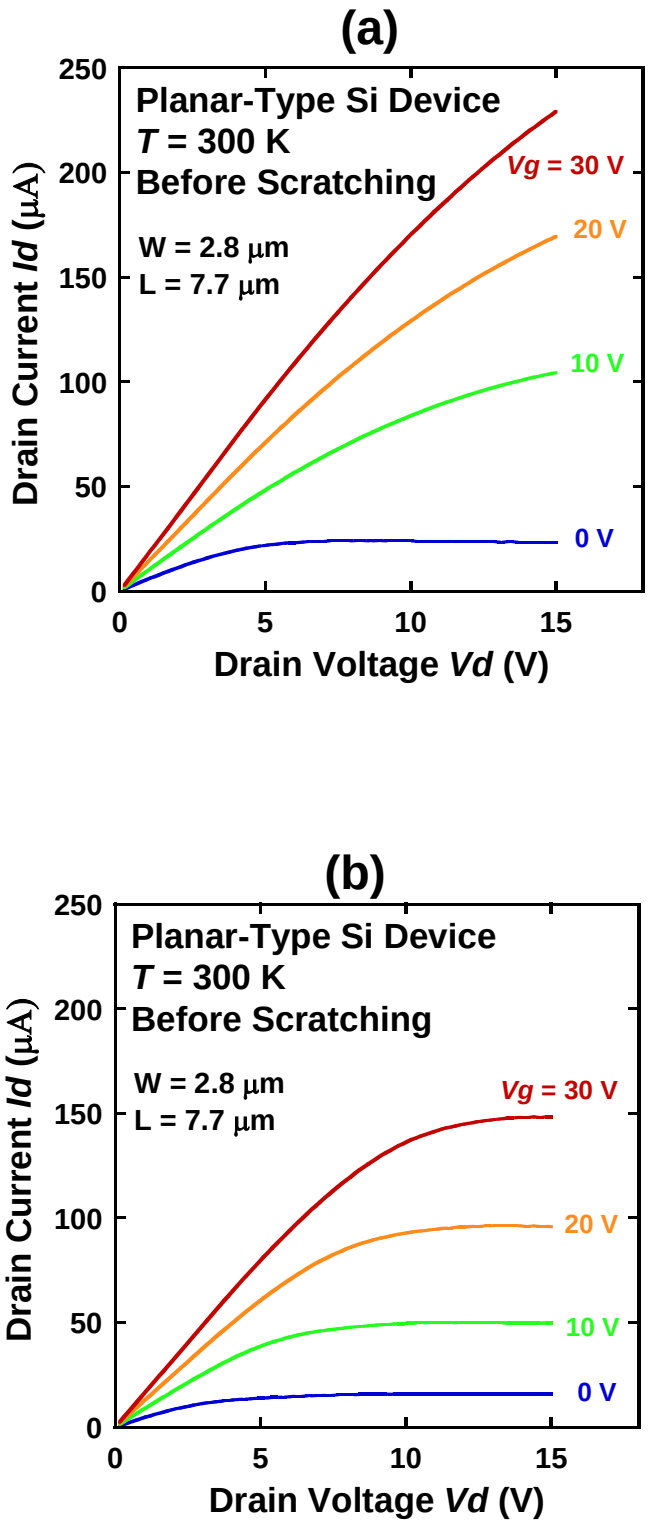


Fig. 5.36. (a) Drain current *Id* of planar-type Si device with various gate voltages as a function of drain voltage *Vd* (a) before and (b) after scratching. (W/L = 0.4)

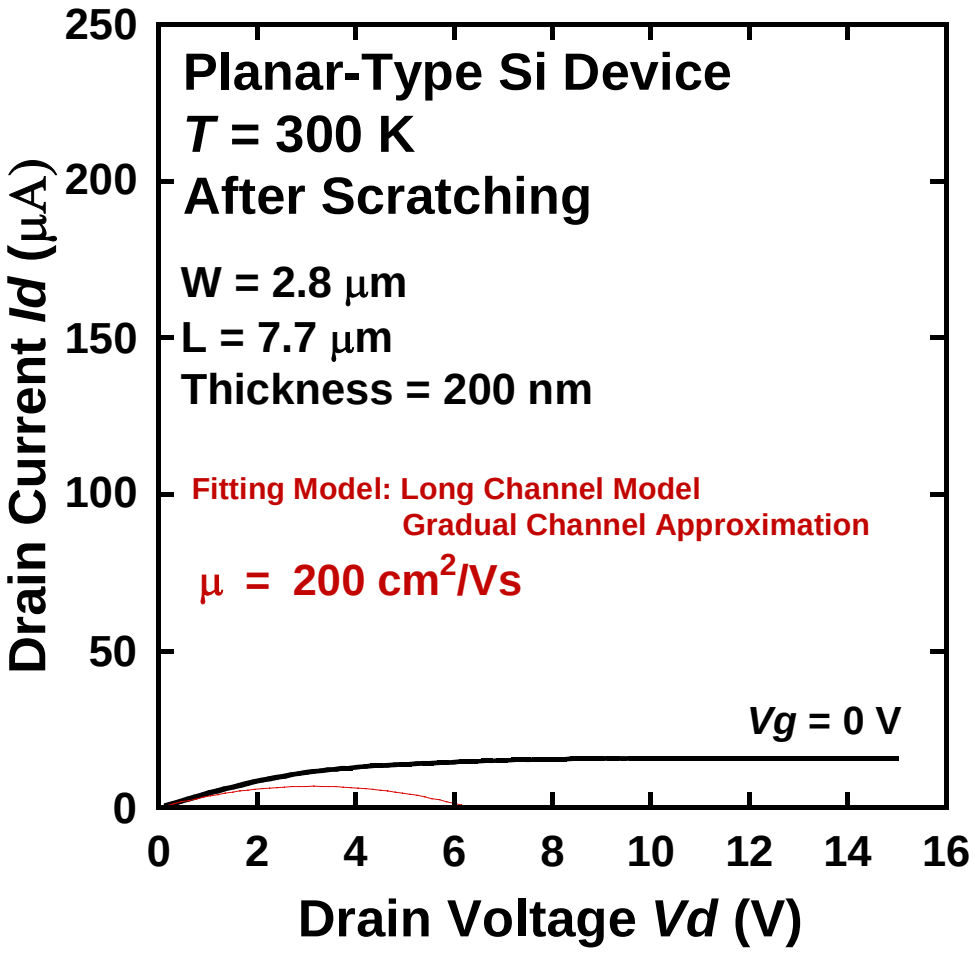


Fig. 5.37. Drain current *Id* of planar-type Si device with gate voltages of 0 V as a function of drain voltage *Vd*. (W/L = 0.4) The model with gradual channel approximation at μ = 200 $cm^2/V \cdot s$ is fitted to experimental data.

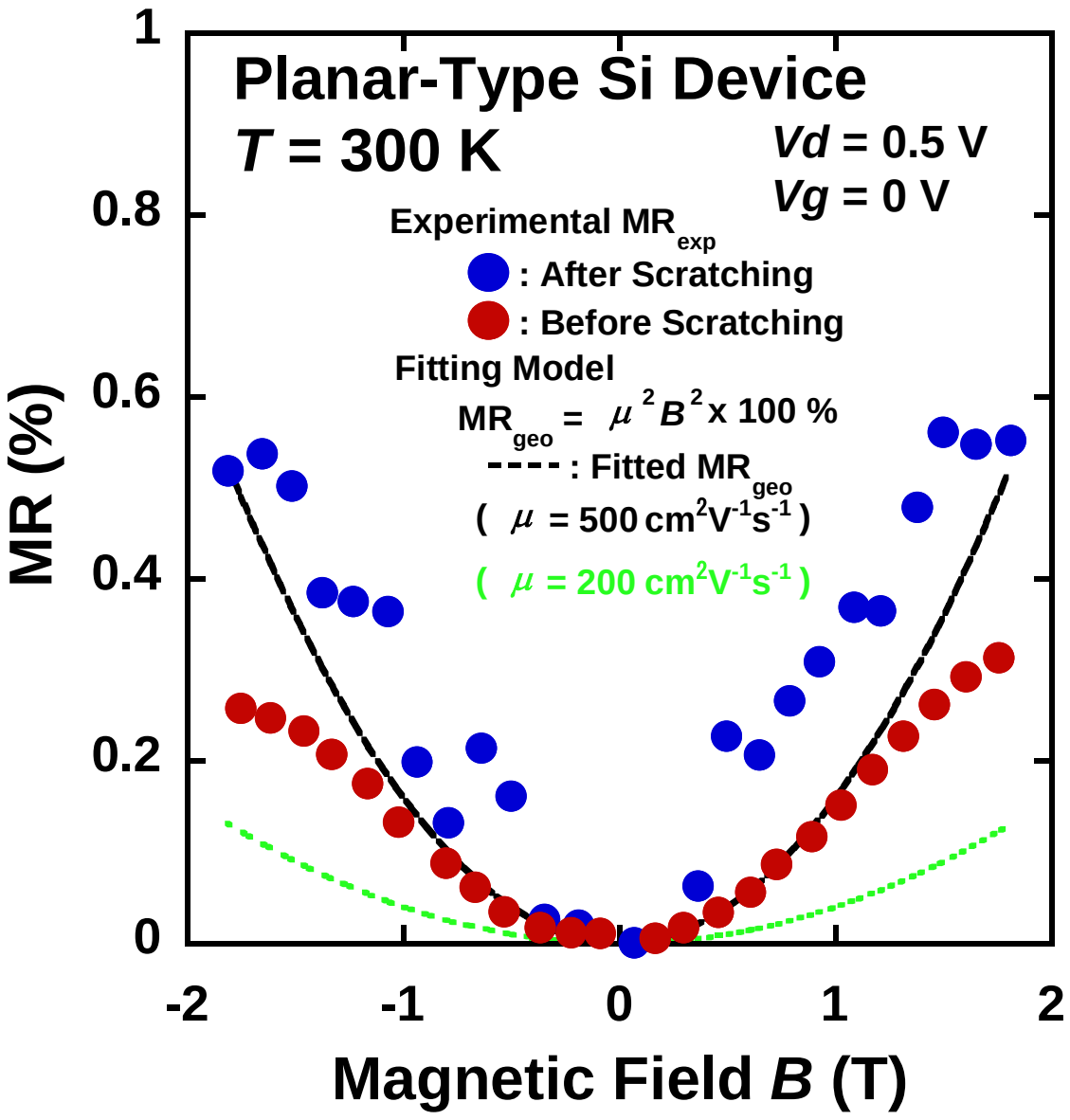


Fig. 5.38. MR of planar-Type Si Device as a function of magnetic field *B* at 300 K. (W/L = 0.4)

5.6 Summary

SPM scratching nanolithography was applied to Si nanochannels for control of device properties of planar-type Si devices. Furthermore, SPM scratching nanolithography was also performed to observe the QPC in Au nanochannels of planar-type devices with in-situ measurement. The conductance of Si and Au channel is easily controlled by SPM scratching lithography. Furthermore, MR effects of planar-type Si devices before and after scratching are investigated. The MR observed in the experiments (MR_{exp}) is MR_{exp} = 0.5 %, which is about 5 times larger than that of the MR induced by the geometrical effect. Therefore, it is suggested that the MR of the planar-type Si devices may arise from physical MR effects, such as the impact ionization of carriers and space charge effect, with the combination of the geometrical MR effect.

Chapter 6

General Conclusions

6.1 SPM Local Oxidation Lithography at Micro- and Nano-Scales

By optimizing the control parameters such as applied bias voltage to the tip, scanning speed of the tip and oscillation amplitude of the cantilever, the fabrication of Si oxide wires with sub-10 nm dimensions was achieved. The average width and minimum FWHM of the Si oxide wire were 9.8 nm and 8.5 nm, respectively.

Furthermore, the throughput of 10 micrometer-scale SPM local oxidation was enhanced almost linearly with the scanning speed, and reached about 10^3 $\mu m^2/s$, which is about 10^5 times larger than that of conventional SPM local oxidation. These results suggest that this method could be a key technique for the fabrication of nanometer-scale devices with micrometer-scale dimensions.

6.2 Scratch Nanolithography Using Scanning Probe Microscopy

In a simple and reliable technique for nanoscale patterning of Si surface using SPM scratching with a diamond-coated tip was performed. The influence of scan parameters on groove size was systematically investigated. The groove size was precisely controlled by the applied force, scan direction and scan cycle. The minimum width of 10 nm was obtained on Si surfaces. There was no effect of the scan speed on the groove size. These results show the possibility of high speed nanolithography on Si surface using SPM scratching. Furthermore, the line and space patterns with a pitch of 30 nm and dot arrays with a density of 2.6×10^{10} cm^{-2} were successfully fabricated. Thus, nanoscale mechanical patterning of Si surface could be realized using SPM. The results imply that SPM scratching with a diamond tip allows

nanoscale patterning of Si surface to be performed simply, and is particularly well suited for the fabrication of nanoscale devices such as single-electron transistors, quantum computing elements and nanophotonic devices.

6.3 Si Nanoscale Devices Fabricated by SPM Lithography Techniques

SPM scratch nanolithography is used for the control of the conductance of planar Si devices. The results show that the conductance of the Si channel is easily controlled by the SPM scratching. Furthermore, SPM scratching nanolithography was applied to Au nanochannels for control of device properties of planar-type devices with in-situ measurement. The conductance plateau was clearly observed below 12 G_0. These results suggested that the electrical properties of planar-type devices are easily controlled by SPM scratch nanolithography techniques.

Furthermore, MR effects in planar-type Si devices are also investigated at 300 K. MR of 15 % is observed in SOI substrate at 300 K, and then, the MR of planar-type Si devices is measured at 1 %. Furthermore, SPM nanoscratching lithography may be able to control MR effects in planar-type Si devices at 300 K.

6.4 Summary

Simple and easy nanolithography techniques for fabrication of nanometer-scale devices using SPM lithography are investigated, and advanced Si based planar type devices with control of electrical properties such as conductance and MR effects. In SPM lithography, by optimizing the control parameters such as applied bias voltage to the tip, scanning speed of the tip and oscillation amplitude of the cantilever, the fabrication of Si oxide and grooves with sub-10 nm resolution was achieved. Furthermore, electrical properties of planar-type devices

are easily controlled by SPM scratch nanolithography techniques. The MR effects of planar-type Si devices are observed at the value of 1 %. Additionally, SPM nanoscratching lithography may be able to control MR effects in planar-type Si devices.

Appendix

Magnetoresistive Effects in Si Substrates and Discrete Si Devices

A.1 Introduction

A magnetic field sensor is an entrance transducer that converts a magnetic field into an electronic signal. Magnetoresistance (MR) effects in ferromagnetic tunnel junctions have generated considerable interest due to their application in magnetic data storage and memory devices [1, 2]. Additionally, tunnel magnetoresistance (TMR) ratio of around 200 % was experimentally realized at room temperature in the Fe(Co)/MgO/Fe(Co) magnetic tunnel junctions [3-4]. Thus, the application of magnetic tunnel junctions has become a key issue in the development of spintronics. Recently, large TMR of 1056% at room temperature has been realized in MgO based double barrier magnetic tunnel junction [5]. Moreover, spin-transistors using an ordinary metal-oxide-semiconductor field-effect-transistor (MOSFET) and magnetic tunnel junctions are proposed [6].

In contrast, research on magnetotransport of semiconductors without using magnetic materials is a field of increasing interest. Recently, nonmagnetic materials such as InSb exhibit geometric MR, which is orders of magnitude larger than the physical MR of other materials [7]. Furthermore, large positive MR effects were also reported in several nonmagnetic semiconductors such as Au/semi-insulating GaAs Schottky diode [8] and B-doped Si [9] MnSb granular films [10]. It is considered that these behaviors are caused by a magnetic-field-controlled impact ionization of carriers. In 2009, it has been found that P-doped Si shows a large positive MR between 0 and 3 T of more than 1,000 % at 300 K and 10,000 % at 25 K [11]. This phenomenon can be explained by the quasi-neutrality breaking of

the space-charge effect, where insufficient charge is present to compensate the electrons injected into the device [12, 13].

The observation of a large MR in Si, based on this phenomenon, is an important milestone towards new spintronics applications. Actually, for sensing application, there is a Corbino disk which consists of InSb with high electron mobility of 78000 $cm^2/V \cdot s$ [14]. With the aim towards its application to electronic devices, the MR of a two-dimensional electron gas in a disordered Si (metal-oxide-semiconductor field-effect-transistor (Si-MOSFET)) system is measured at a magnetic field of 40 T [15]. In this device, the MR of 100 % was obtained since the MR was considered as a result of modified scattering due to screening and density of states modifications caused by the spin polarization of the two-dimensional electron gas [16]. Furthermore, Si-MOSFET structures exhibit a positive MR of about 18 % at room temperature with a magnetic field of 9 T, due to the presence of high-mobility electrons in the Si inversion layer [17]. Moreover, MR measurements were performed on n-type Si MOS field-effect transistors (FET), and this device exhibits 12 % of MR at 300 K under the magnetic field of 10 T [18]. Figure A.1(a) shows the comparison of these MR effects in various materials. Furthermore, the MR of these nonmagnetic materials and devices are plotted in Fig. A.1(b).

To investigate the MR of the Si-MOSFET structure in detail, discrete Si transistors are one of the suitable candidates since these discrete devices with FET geometries have stable and uniform electrical properties. Additionally, they are inexpensive and high-quality products. In this dissertation, we investigate of MR properties of silicon substrates and discrete Si devices with a magnetic field up to 2.2 T at 300 and 77 K.

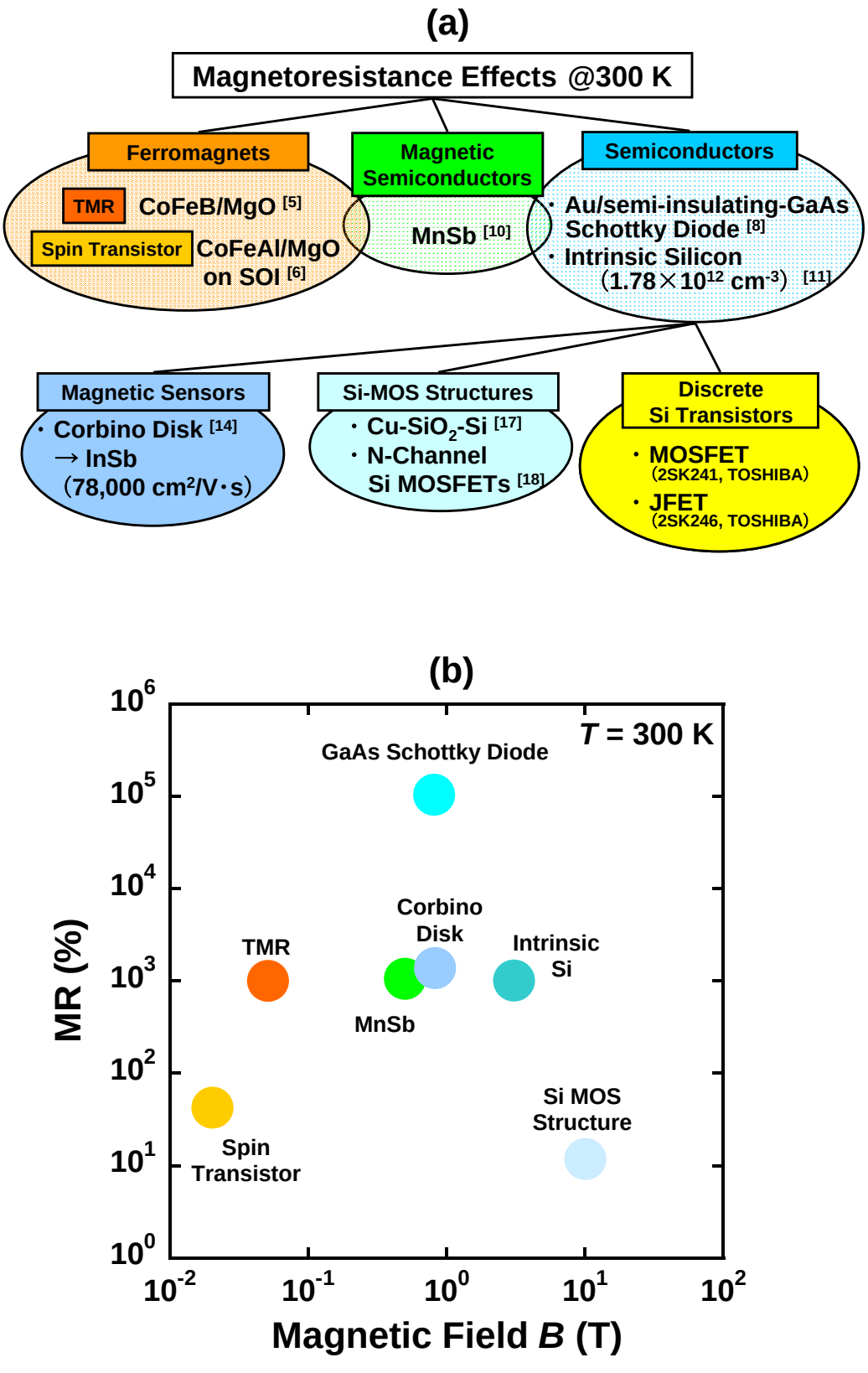


Fig. A.1. (a) Comparison of these MR effects in various materials and devices at room temperature (b) MR of various materials and devices in (a).

A.2 Magnetoresistive Effects in Si Substrates

MR effect of p-type Si substrate with resistivity of 1 kΩcm (thickness = 525 μm) was investigated. Schematic illustrations of the sample and direction of the applied magnetic field *B* are shown in Fig. A.2. The current-voltage (I-V) characteristics were measured at 300K. Figure A.3(a) shows current and MR versus magnetic field characteristics with the applied magnetic field *B* up to 2.6 T. The MR of p-type Si substrate gradually increases with the increase of magnetic field, reaching 9 % of MR at the magnetic field of 2.6 T. Here, the theoretical transverse MR is estimated at the hole and electron mobility of 10^{13} and 10^{142} cm^{-3}, respectively. Transverse MR is one of the galvanomagnetic effects, in which a magnetic field perpendicular to an electric current gives rise to an electrical potential change in the direction of the current. From the Fig, A.3(b), experimental MR is larger than the theoretical transverse MR. These results indicate that the MR effects of p-type Si substrate are induced by physical phenomena such as space charge effects or impact ionization of carriers.

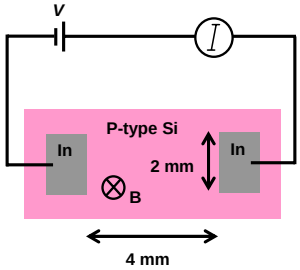


Fig. A.2. Schematic illustration of the devices structure and measurement set-up. Device length and width is 4 and 2 mm, respectively.

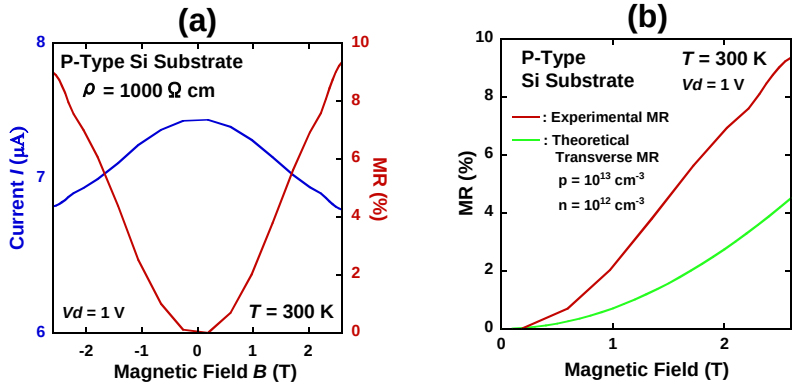


Fig. A.3. (a) Current and MR versus magnetic field characteristics with the applied magnetic field *B* up to 2.6 T. (b) MR dependences of p-type Si substrate on the magnetic field as compared with transverse MR induced by galvanomagnetic effects.

A.3 Magnetoresistive Effects in Discrete Si P-N Junction Diodes

MR effect of p-n Si diode was investigated. Photograph and the experimental set up are shown in Fig. A.5(a) and (b). The current-voltage (I-V) characteristics were measured at 300 and 77 K. Here, MR is defined as $(R(B)/R(0) - 1) \times 100$ %, where $R(B)$ and $R(0)$ are the resistances at an applied magnetic field B and zero, respectively.

Figure A.6(a) shows current and MR versus voltage characteristics of the p-n Si diode with the applied magnetic field B of 0 and 2.6 T at 300 K. The MR of p-n Si diode is 2 % above voltage of 0.4 V. The MR dependences of the p-n Si diode on the magnetic field were also measured in the Fig. A.6(b). As shown in the figure, MR is enhanced with increase of the magnetic field. These MR characteristics are consistent with the result of IV and MR properties in Fig. A.6(a).

Furthermore, MR of the p-n Si diode is measured at the temperature of 77 K. The current is drastically suppressed at 77 K, and MR of 120 % is observed as shown in Fig. A.7(a) and (b). Moreover, MR dependences of the p-n Si diode on the magnetic field with various voltages from 1.07 to 1.25 V were investigated as shown in Fig. A.8. Form the figure, MR is well controlled by the voltages. These results show the MR effect also occurred in p-n Si diode.

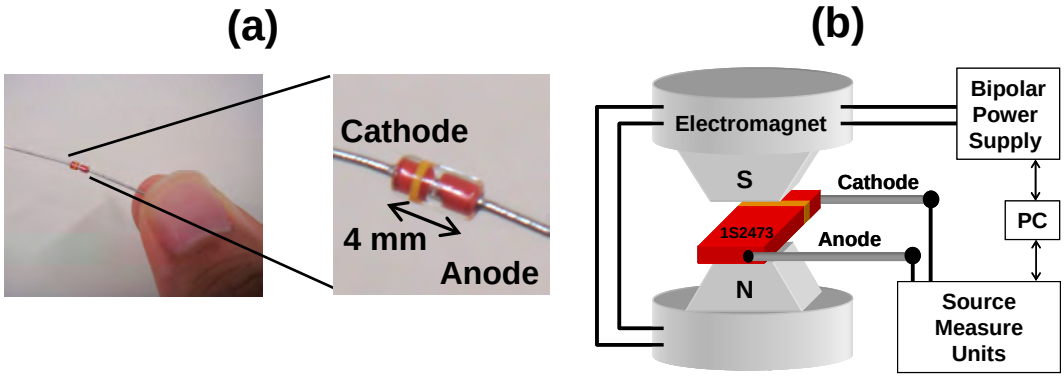


Fig. A.5. (a) Photograph of p-n diode (1S2473, ROHM). (b) Schematic of p-n diode and direction of applied magnetic field B.

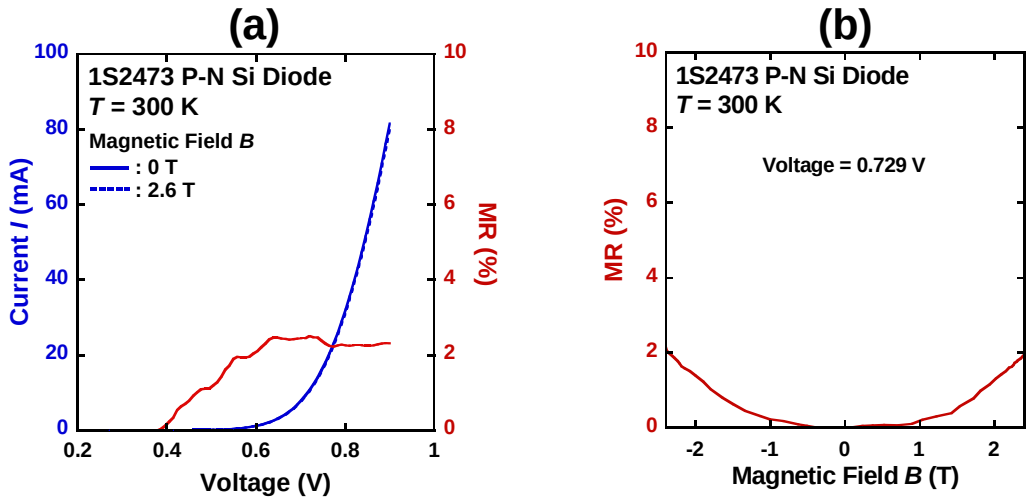


Fig. A.6. (a) Current and MR versus voltage characteristics of the p-n Si diode with the applied magnetic field B of 0 and 2.6 T at 300 K. (b) MR dependences of the p-n Si diode on the magnetic field with the voltage of 0.729 V.

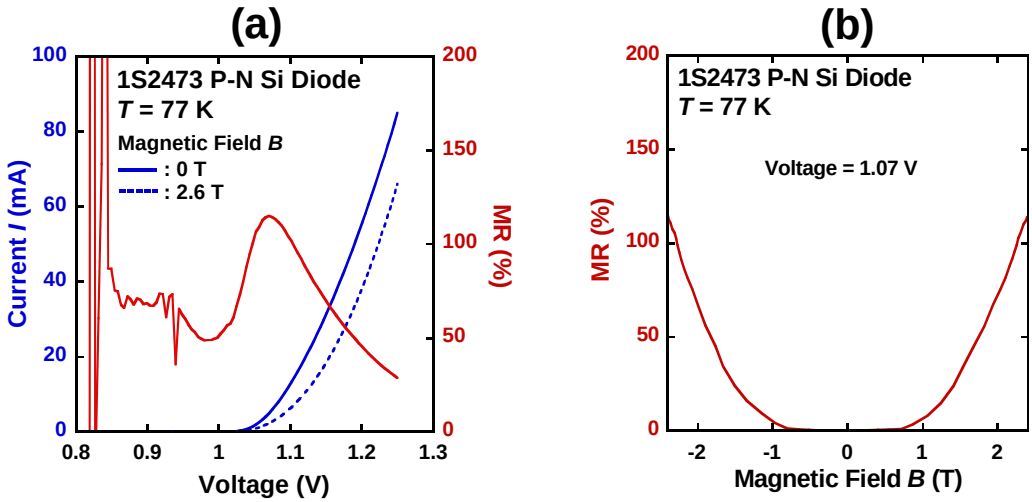


Fig. A.7. (a) Current and MR versus voltage characteristics of the p-n Si diode with the applied magnetic field B of 0 and 2.6 T at 77 K. (b) MR dependences of the p-n Si diode on the magnetic field with the voltage of 1.07 V.

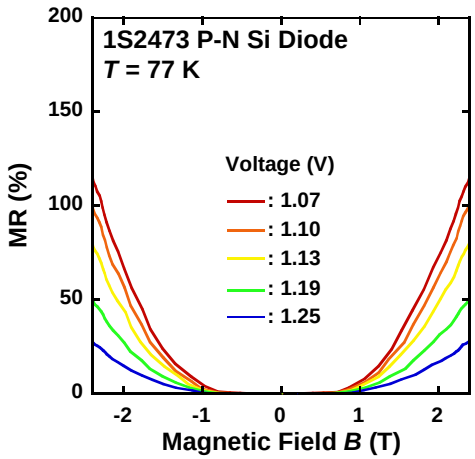


Fig. A.7. MR dependences of the p-n Si diode on the magnetic field with various voltage from 1.07 to 1.25 V.

A.4 Magnetoresistive Effects in Discrete Si Transistors

A.4.1 Si N-Channel MOSFETs

Si n-channel normally-on MOSFETs (2SK241, TOSHIBA) were studied to investigate the MR effects in discrete Si transistors. Schematic illustrations of the devices and direction of the applied magnetic field *B* are shown in Fig. A.9. Although device parameters such as gate length *L*, gate width *W* and electron mobility μ are unknown, the maximum drain current ratings of the MOSFET (drain voltage *Vd* = 10 V and gate voltage *Vg* = 0 V) are 7 mA. The current-voltage (I-V) characteristics were measured at 300 and 77 K. Here, MR is defined as $(R(B)/R(0) - 1) \times 100$ %, where $R(B)$ and $R(0)$ are the resistances at an applied magnetic field *B* and zero, respectively.

Figure A.10(a) shows drain current *Id* versus drain voltage *Vd* characteristics of the MOSFET with the applied magnetic field *B* of 0 and 2.2 T at 300 K. Gate voltages *Vg* ranging from -0.25 to -0.65 V are also applied to the sample. When a negative gate bias is applied to the MOSFET, a typical gate-modulated n-channel MOSFET behavior is observed, as shown in Fig. A.10(a). From the figure, the drain currents at various gate voltages are suppressed in the magnetic field of 2.2 T. Figure A.10(b) shows the MR of the MOSFET as a function of drain voltage. As shown in figure, the MR of the MOSFET is about 8 % with the gate voltage of -0.25 V. Figure A.11(a) shows typical drain current versus gate voltage transfer characteristics of the MOSFET for various drain voltages ranging from 5 to 200 mV at 300 K. As the drain voltage is increased from 5 to 200 mV, the drain current gradually increases. From the figure A.11(b), the MR of the MOSFET shows values of 8 % over the gate voltage of about -0.4 V, which is consistent with the result of MR-*Vd* properties in Fig. A.10(b). Here, MR of the MOSFET below -1.0 V of the gate voltage is not expressed due to the current detection limit of the measurement system.

Figure A.12(a) indicates the drain current in the magnetic fields of 0 and 2.2 T as a function of drain voltage when gate voltages are applied to the MOSFET at 77 K. Drain currents are drastically suppressed and MR as shown in Fig. A.12(b) is obviously enhanced at 77 K as compared with that at 300 K. Figure A.13(a) also shows drain current of the MOSFET as a function of gate voltages at several drain voltages between 5 and 200 mV at 77 K. Furthermore, MR of the MOSFET versus gate voltages at 77 K is also plotted in Fig. A.13(b). The MR of the MOSFET at 77 K is reached about 60 % and clearly tuned by the gate voltages. Additionally, the MR is consistent with the results of the *Id-Vd* measurements shown in Figs. A.12(a). These results indicate that MR of the MOSFET is easily controlled by the gate voltage.

To clarify MR characteristics further, the MR dependences of the MOSFET on the magnetic field were measured. Figures A.14(a) and (b) show the MR of the MOSFET as a function of magnetic field at 300 and 77 K, respectively. The measurement at 300 K was carried out by applying a gate voltage of -0.25 V and a drain voltage of 0.2 V. As shown in the figure, the 300 K MR shows a continuous increase, reaching about 8 % at the magnetic field of 2.2 T. Additionally at 77 K, the MR is clearly enhanced to be 55 % when a drain voltage Vd = 0.2 V is applied to the devices with a gate voltage Vg = 0 V.

In the presence of a magnetic field aligned perpendicular to the current flow plane, the conductivities of the two-dimensional electron gas are expressed as follows,

$$\begin{aligned} j_x &= \sigma_{xx} E_x + \sigma_{xy} E_y, \\ j_y &= -\sigma_{xy} E_x + \sigma_{xx} E_y, \end{aligned} \tag{A.1}$$

where E_x and E_y are the electric fields in the x and y planes, respectively [19]. Furthermore, σ_{xx} and σ_{xy}, which are the components of the conductivity tensor, are also described as follows [18],

$$\begin{aligned} \sigma_{xx} &= \sigma_0 /(1+\mu^2 B^2), \\ \sigma_{xy} &= \sigma_0 \mu B /(1+\mu^2 B^2). \end{aligned} \tag{A.2}$$

where B is the magnetic field, μ is the electron mobility and $\sigma_0 = n_s e\mu$ with n_s and e being the sheet carrier concentration and charge, respectively. In the case of a very short and wide device ($L \ll W$, where L is the length in the direction of the current flow and W is the width of the device), the Hall voltage is short circuited by long current-supplying contacts, resulting in

$$E_y = 0, \tag{A.3}$$

then, the current density in the x direction at the magnetic field B is expressed as

$$j_x = \sigma_{xx} E_x = \sigma_0 / (1 + \mu^2 B^2) \cdot E_x. \tag{A.4}$$

Additionally, the resistivity ρ_0 (0) at the magnetic field of 0 T is defined as

$$\rho_0(0) = 1/\sigma_0. \tag{A.5}$$

Therefore, the resistivity ρ_0 (B) in the presence of the magnetic field B is expressed as

$$\rho_0(B) = \rho_0(0) \cdot (1 + \mu^2 B^2). \tag{A.6}$$

Finally, the MR induced by a geometrical effect (MR_{geo}) is described as

$$MR_{geo}(\%) = \frac{R(B) - R(0)}{R(0)} \times 100 = \frac{\rho_0(B) - \rho_0(0)}{\rho_0(0)} \times 100 = \mu^2 B^2 \times 100. \tag{A.7}$$

If the MR induced by the geometrical effect occurs and dominates in the MOSFET, the MR of the discrete Si transistors may be expressed as $MR_{geo} = \mu^2 B^2$ x 100 %. As shown in Fig. A.14(a), the MR of the MOSFET is in good agreement with the fitting model ($MR_{geo} = \mu^2 B^2$ x 100 %), where μ is fitted to be 1500 $cm^2V^{-1}s^{-1}$.

Here, the electron mobility and carrier density in the discrete Si transistors are unknown, because the L and W are generally undocumented in the data sheet of the devices [20]. Therefore, the mobility of the discrete Si transistors is not well determined through the electrical properties. However, it is reported that the mobilities of the MOSFET with several gate lengths under a magnetic field at 300 K are below 350 $cm^2V^{-1}s^{-1}$, and the MR of these devices is clearly proportional to the squares of the magnetic field, B^2 [18]. Furthermore, Takagi *et al.* also presented that the electron mobilities of the n-channel MOSFET (W/L =

100/200 μm) with substrate concentrations ranging from 10^{15} to 10^{18} cm^{-3} at 300 K are below 1000 $cm^2V^{-1}s^{-1}$ in the linear region [21]. In addition, the electron mobility of the MOSFET (W/L = 100/10 μm) with the substrate concentration of 5.0 x 10^{16} cm^{-3} is less than 700 $cm^2V^{-1}s^{-1}$ at 300 K [22].

If the electron mobility of the MOSFET investigated in the experiments is considered to be 1000 $cm^2V^{-1}s^{-1}$ at 300 K, the MR induced by the geometrical effect (MR_{geo}) at the magnetic field of 1.5 T is assumed to be MR_{geo} = 2.2 %. However, the MR observed in the experiments (MR_{exp}) is MR_{exp} = 5.4 %, which is about 2.5 times larger than that of the MR induced by the geometrical effect. Furthermore, as shown in Fig. A.14(b), MR of the MOSFET at 77 K is in good agreement with the fitting model, where μ is fitted to be 3500 $cm^2V^{-1}s^{-1}$. Here, the mobility of the MOSFET at 77 K is reported to be about 2500 $cm^2V^{-1}s^{-1}$ [23]. Therefore, if the electron mobility of the MOSFET at 77 K is considered to be the value, assumed MR_{geo} of the MOSFET at the magnetic field of 1.5 T are estimated to be MR_{geo} = 14 %. However, experimental MR_{exp} of the MOSFET are MR_{exp} = 26 %, which is also about 1.9 times larger than assumed MR_{geo}. The summery of MR effects in the MOSFET at the magnetic of 1.5 T are listed in Table A.1. It clearly indicates that enhancement ratio (MR_{exp}/MR_{geo}) of the MOSFET at room temperature becomes almost the same as that at 77 K. Recently, it has been previously discussed by Ciccarelli *et al.* that MR of the Si MOSFET below the threshold voltage at 4.2 K has to be associated with space charge transport regime [24]. Therefore, it is suggested that the MR of the discrete Si transistors may arise from physical MR effects, such as the impact ionization of carriers [8, 10] and space charge effect [11-13], with the combination of the geometrical MR effect.

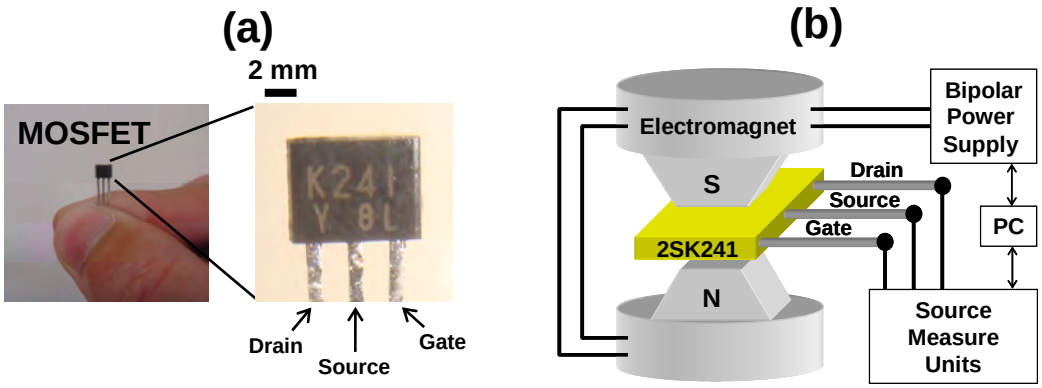


Fig. A.9. (a) Photograph of MOSFET (2SK241, TOSHIBA). (b) Schematic of MOSFET and direction of applied magnetic field *B*.

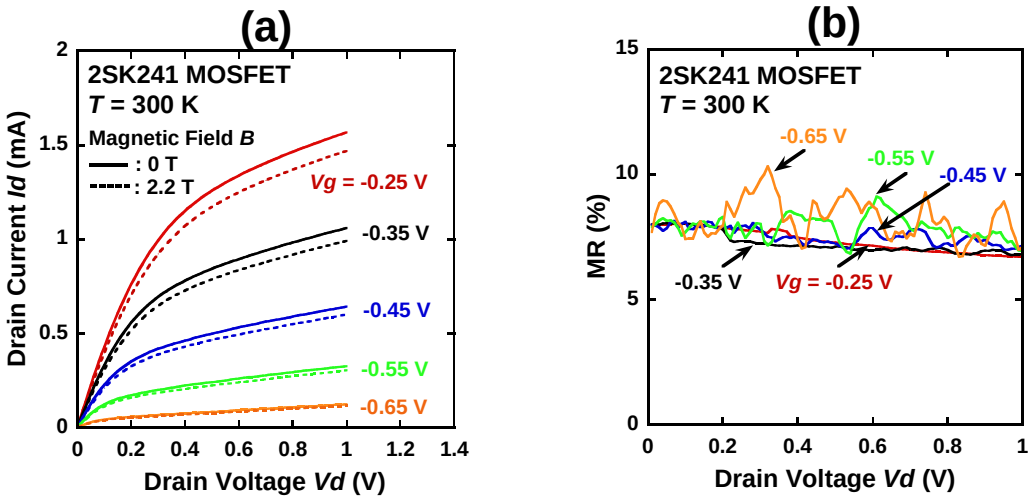


Fig. A.10. (a) Drain current *Id* versus drain voltage *Vd* characteristics of MOSFET with the applied magnetic field *B* of 0 and 2.2 T at 300 K. (b) MR of MOSFET as a function of drain voltage *Vd* at 300 K.

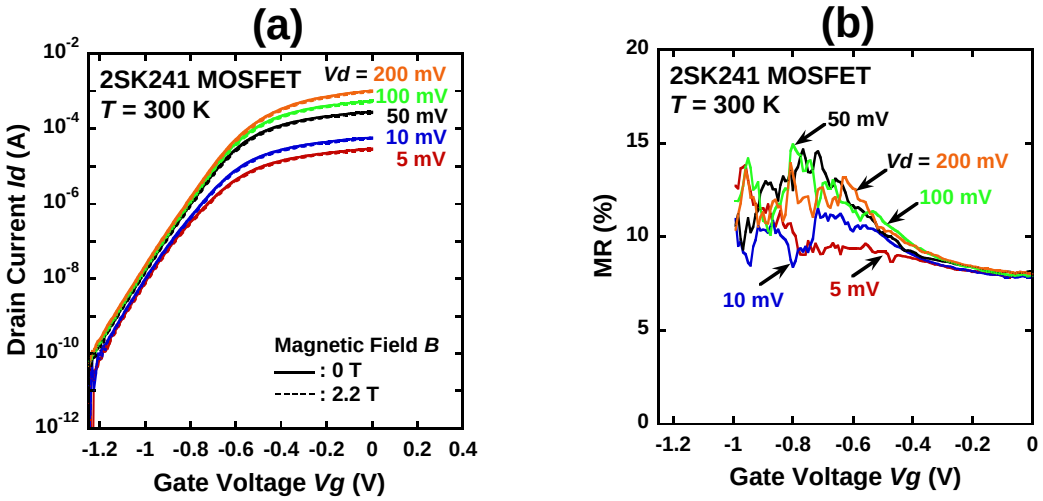


Fig. A.11. (a) Drain current *Id* versus gate voltage *Vg* at various drain voltages *Vd* ranging from 5 to 200 mV with the applied magnetic field *B* of 0 and 2.2 T in MOSFET at 300 K. (b) MR of MOSFET as a function of gate voltage *Vg* at 300 K.

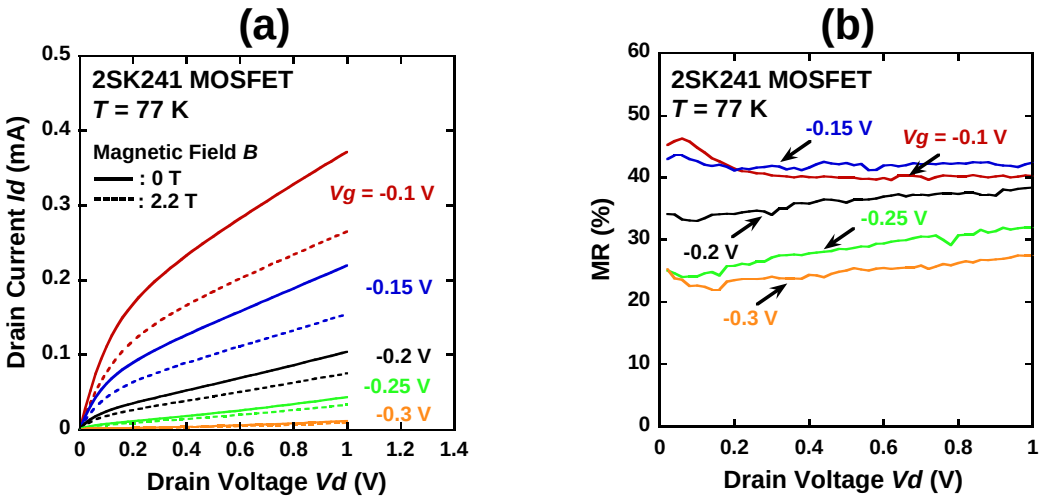


Fig. A.12. (a) Drain current *Id* of MOSFET in the magnetic field *B* of 0 and 2.2 T as a function of drain voltage *Vd* at 77 K. (b) MR dependence of MOSFET on drain voltage *Vd* at 77 K.

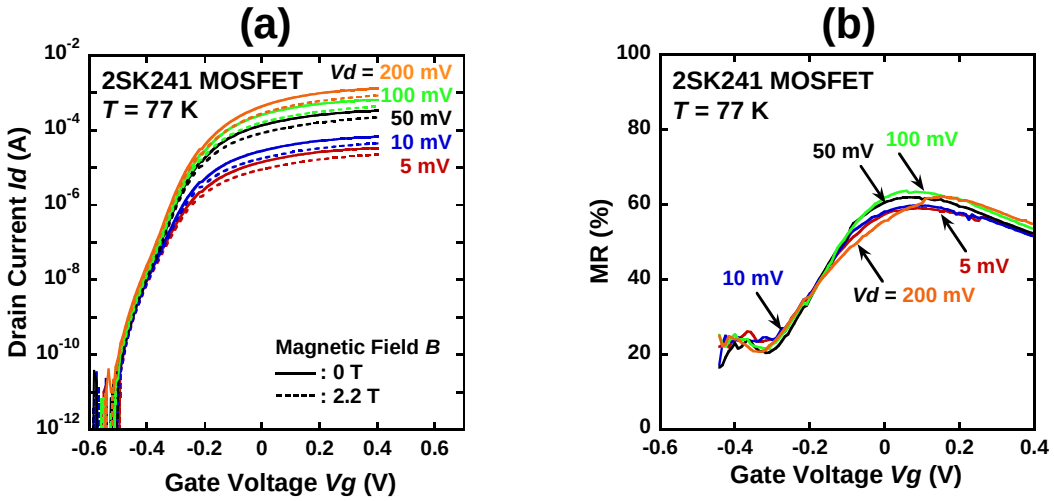


Fig. A.13. (a) Drain current *Id* of MOSFET in the magnetic field *B* of 0 and 2.2 T as a function of gate voltage *Vg* at 77 K. (b) MR dependence of MOSFET on gate voltage *Vg* at 77 K.

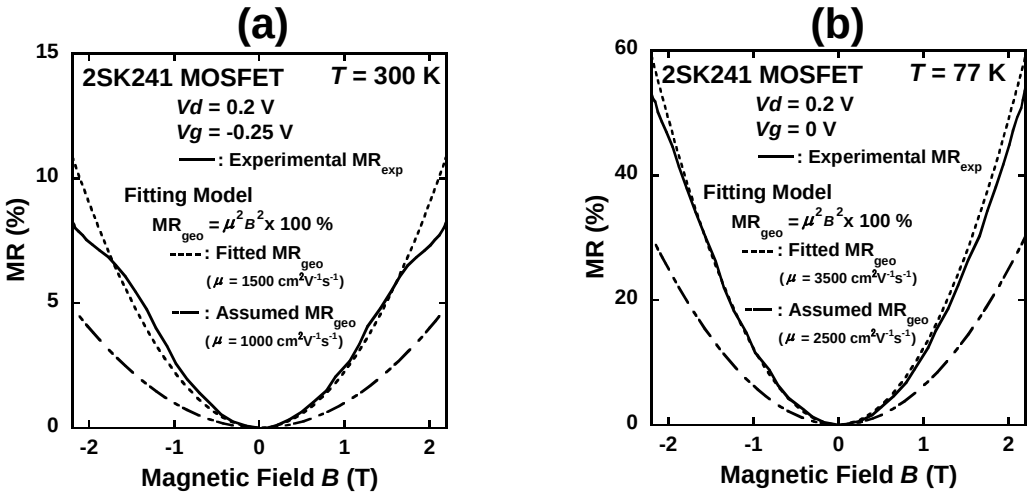


Fig. A.14. MR of MOSFET as a function of magnetic field *B* at (a) 300 and (b) 77 K.

Table A.1. Comparison of MR effects in MOSFET (2SK241, TOSHIBA) at 300 and 77 K with magnetic field of 1.5 T.

Temperature (K)	Experimental MR_{exp} (%)	Fitted MR_{geo} (%)	Fitted Mobility ($cm^2/V \cdot s$)	Assumed MR_{geo} (%)	Assumed Mobility ($cm^2/V \cdot s$) [Ref]	Enhancement Ratio
300	5.4	5.1	1500	2.2	1000 [21]	2.5
77	26	27	3500	14	2500 [23]	1.9

A.4.2 Si N-Channel Junction FETs (JFETs)

In the experiments, the MR of normally-on n-channel JFETs (2SK246, TOSHIBA) is measured. The experimental set-up is shown in Fig. A.15, which is the same at the MOSFET experiment. The magnetic field *B* of up to 2.2 T was applied to the sample as shown in Fig. A.15. The maximum drain current ratings of the JFET (drain voltage *Vd* = 10 V and gate voltage *Vg* = 0 V) are 3 mA from the data sheet [25].

Figure A.16(a) also shows drain current *Id* versus drain voltage *Vd* characteristics of the JFET with the applied magnetic field *B* of 0 and 2.2 T at 300 K. Gate voltages *Vg* ranging from 0 to -0.7 V are also applied to the sample. From the figure, the drain currents at various gate voltages are also suppressed in the magnetic field of 2.2 T. As shown in Fig. A.16(b), the MR of the JFET is about 15 % with the gate voltage of -0.25 V. Figures A.17(a) show drain current versus gate voltage transfer characteristics of the JFET for various drain voltages ranging from 5 to 200 mV at 300 K. The MR of the JFET at 300 K is also shown in Figs. A.17(b). From the figure, the MR of the JFET shows values of 15 % over the gate voltage of about -1.2 V.

Figure A.18(a) shows *Id*-*Vd* characteristics at 77 K. Drain currents with various gate voltages are drastically suppressed as compared with that at 300 K. In addition, as shown in Fig. A.18(b), MR at the drain voltage of 0.2 V is clearly enhanced to be about 230 % with the gate voltage of -0.25 V. Figure A.19(a) shows drain current as a function of gate voltage in the JFET at 77 K. The MR of the JFET versus gate voltage at 77 K is also shown Figs. A.19(b). The MR at 77 K is enhanced from 50 to 230 % with varying the gate voltage from -1.0 to -0.3 V. Additionally, the MR of the JFET is consistent with the results of the *Id*-*Vd* measurements shown in Figs. A.18(a) and (b). These results indicate that MR of the JFET is also easily controlled by the gate voltage.

Furthermore, the MR dependences of the JFET on the magnetic field were measured at 300 and 77 K as shown in Figs. A.20(a) and (b), respectively. As shown in the figures, when a drain voltage *Vd* = 0.2 V is applied to the JFET with a gate voltage *Vg* = -0.25 V at 300 K, the MR shows a continuous increase, reaching about 15 % at the magnetic field of 2.2 T. Additionally at 77 K, the MR (*Vd* = 0.2 V, *Vg* = 0 V) is clearly enhanced to be 252 %.

The MR induced by the geometrical effect is mentioned in MOSFET experiments. If the same MR effect occurred in JFET, the geometrical MR of JFET may be also expressed as $MR_{geo} = \mu^2 B^2$ x 100 %. As shown in Fig. A.20(a), the MR of the JFET is in good agreement with the fitting model ($MR_{geo} = \mu^2 B^2$ x 100 %), where μ is fitted to be 1800 $cm^2V^{-1}s^{-1}$. In case of the JFET, it is known that the electron mobility of the discrete JFET (SNJ450) is estimated to be 1260 $cm^2V^{-1}s^{-1}$ at 300 K [26].

If the electron mobility of the JFET investigated in the experiments is considered to be 1260 $cm^2V^{-1}s^{-1}$, the MR induced by the geometrical effect (MR_{geo}) at the magnetic field of 1.5 T is assumed to be MR_{geo} = 3.5 %. However, the MR observed in the experiments (MR_{exp}) is MR_{exp} = 8.5 %, which is about 2.4 times larger than that of the MR induced by the geometrical effect. Furthermore, as shown in Fig. A.20(b), MR of the JFET at 77 K is in good agreement with the fitting model, where μ is fitted to be 7500 $cm^2V^{-1}s^{-1}$. Here, mobility of discrete JFET (2N3823) at 77 K is investigated to be below 5000 $cm^2V^{-1}s^{-1}$ [27]. Therefore, if the electron mobility of the JFET at 77 K is considered to be 5000 $cm^2V^{-1}s^{-1}$, assumed MR_{geo} of the JFET at the magnetic field of 1.5 T are estimated to be MR_{geo} = 56 %. However, experimental MR_{exp} of the JFET are MR_{exp} = 125 %, which is also about 2.2 times larger than that of assumed MR_{geo}. The summery of MR effects in the JFET at the magnetic of 1.5 T are listed in Table A.2. It clearly indicates that enhancement ratio (MR_{exp}/MR_{geo}) of the JFET at room temperature becomes almost the same as that at 77 K.

In the FET geometries, the gate width and gate length may be different between the MOSFET and the JFET, resulting in the difference of the magnitude of geometrical MR effect between both transistors. However, the MOSFET and JFET experimentally show the MR_{exp} is approximately 1.9 ~ 2.5 times larger than assumed MR_{geo} induced by the geometrical MR effect. These results also imply that the MR of the discrete Si transistors may arise from physical MR effects with the combination of the geometrical MR effect.

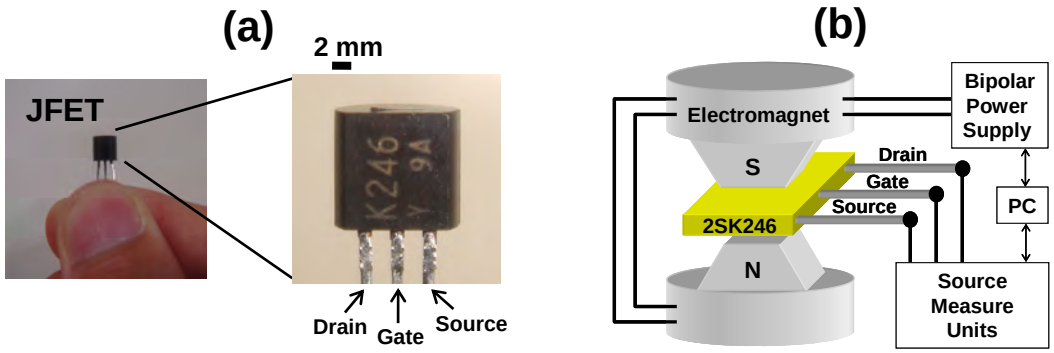
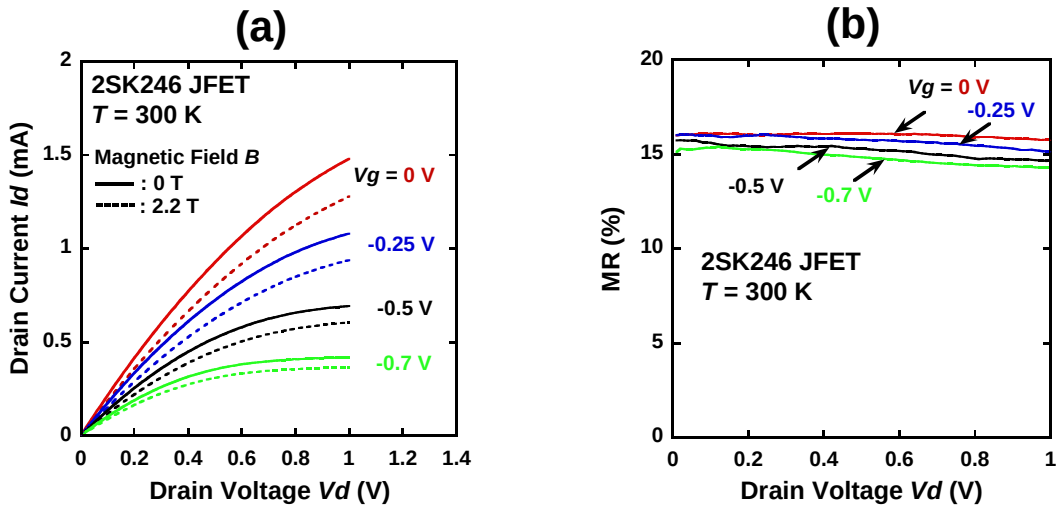


Fig. A.15. (a) Photograhph of JFET (2SK246, TOSHIBA). (b) Schematic of JFET and direction of applied magnetic field *B*.



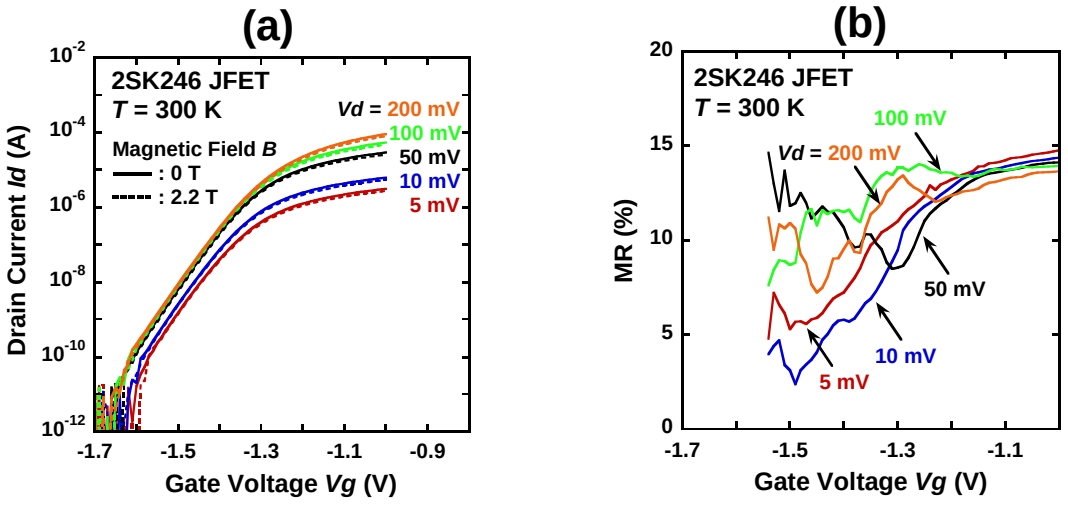


Fig. A.17. (a) Drain current *Id* versus gate voltage *Vg* at various drain voltages *Vd* ranging from 5 to 200 mV with the applied magnetic field *B* of 0 and 2.2 T in JFET at 300 K. (b) MR of JFET as a function of gate voltage *Vg* at 300 K.

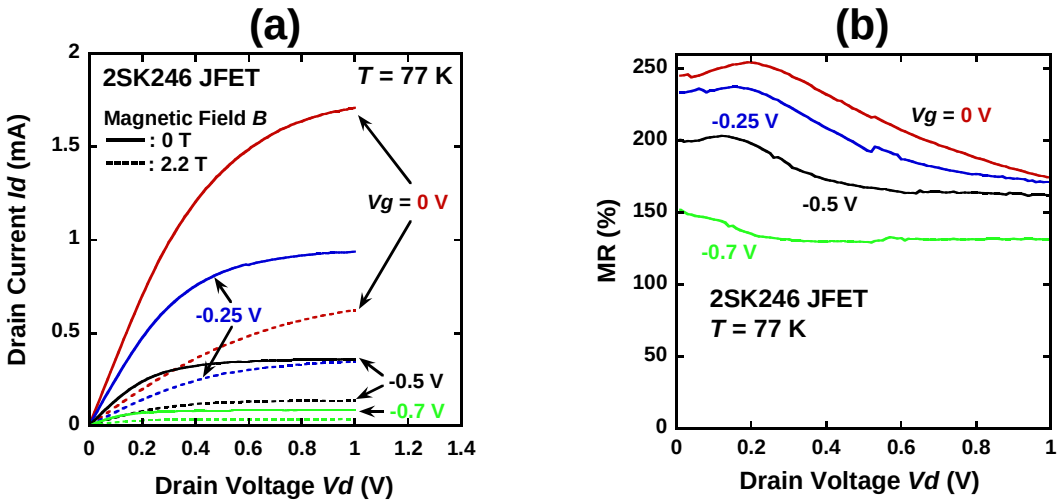


Fig. A.18. (a) Drain current *Id* of JFET in the magnetic field *B* of 0 and 2.2 T as a function of drain voltage *Vd* at 77 K. (b) MR dependence of JFET on drain voltage *Vd* at 77 K.

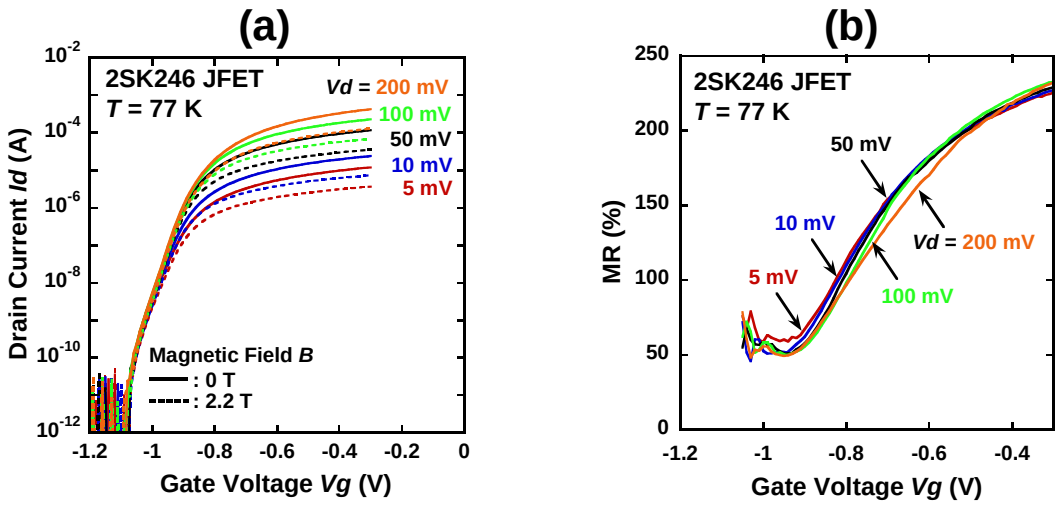


Fig. A.19. (a) Drain current *Id* of JFET in the magnetic field *B* of 0 and 2.2 T as a function of gate voltage *Vg* at 77 K. (b) MR dependence of JFET on gate voltage *Vg* at 77 K.

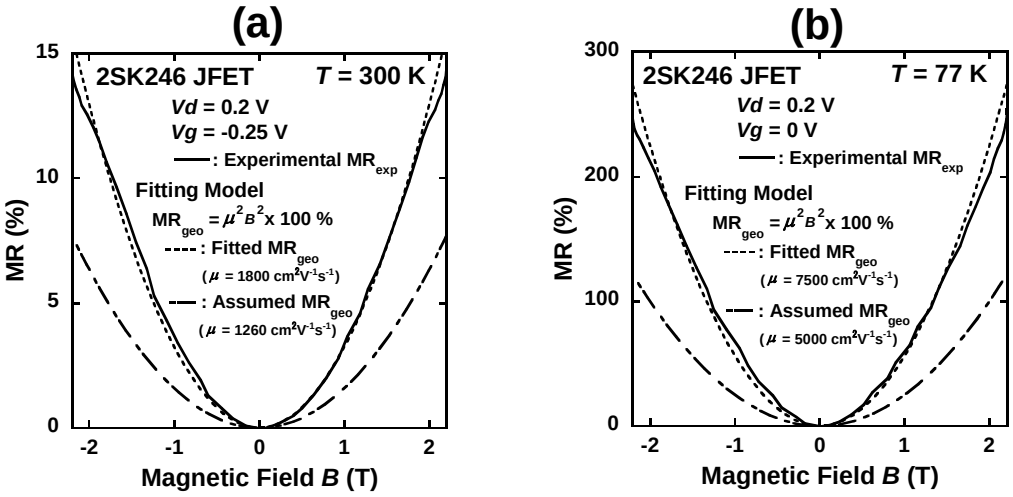


Fig. A.20. MR of JFET as a function of magnetic field *B* at (a) 300 and (b) 77 K.

Table A.2. Comparison of MR effects in JFET (2SK246, TOSHIBA) at 300 and 77 K with magnetic field of 1.5 T.

Temperature (K)	Experimental MR_{exp} (%)	Fitted MR_{geo} (%)	Fitted Mobility ($cm^2/V \cdot s$)	Assumed MR_{geo} (%)	Assumed Mobility ($cm^2/V \cdot s$) [Ref]	Enhancement Ratio
300	8.5	7.3	1800	3.5	1260 [26]	2.4
77	125	126	7500	56	5000 [27]	2.2

A.4.3 Si NPN Bipolar Transistors

In the experiments, Si npn bipolar (2SC4116, TOSHIBA) were studied to investigate the MR effects. The outer packages of the devices are shown in Figs. A.21(a). Schematic illustrations of the devices and direction of the applied magnetic field *B* are shown in Fig. A.21(b). As shown in Fig. A.22(a) and (b), two types configuration is performed for the measurements of MR effect in npn bipolar transistors. One is common-emitter and the other is common-base configuration. In addition, MR is also defined as $(R(B)/R(0) - 1)\times 100$ %, where $R(B)$ and $R(0)$ are the resistances at an applied magnetic field *B* and zero, respectively.

Figure A.23(a) shows collector current I_C versus collector voltage V_{CE} characteristics of the bipolar transistor in the common-emitter with the applied magnetic field *B* of 0 and 2.5 T. Base current I_b ranging from 250 to 50 μA are applied to the sample. From the figure, the collector currents at various base currents are suppressed in the magnetic field of 2.5 T. Figure A.23(b) shows the MR of the bipolar transistor as a function of collector voltage. As shown in figure, the MR of the bipolar transistor is about 2 %. Figure A.24(a) also shows collector current I_C versus collector voltage V_{CE} characteristics of the bipolar transistor at the low collector voltage. MR as shown in Fig. A.24(b) is clearly enhanced at about 0 A of the collector current.

Furthermore, typical collector current versus base current transfer characteristics of the bipolar transistor for various collector voltages ranging are shown in Fig. A.25(a). From the figure A.25(b), the MR of bipolar transistor at the active region is 2 %, which is consistent with the result of MR-V_{CE} properties in Fig. A.23(b).

Figure A.26, A.27, and A.28 show the MR measurements at 77 K. Collector currents are drastically suppressed and MR as shown in Fig. A.26(b) and 28(b) is obviously enhanced at 77 K as compared with that at 300 K.

To clarify MR characteristics further, the MR dependences of the bipolar transistor on the magnetic field were measured. Figures A.29(a) and (b) show the MR of the bipolar transistor as a function of magnetic field at 300 K. As shown in the figure, the 300 K MR shows a continuous increase, reaching about 2500 % at the magnetic field of 2.5 T. Additionally in the common-base configuration, this MR property is quite similar to that of common-emitter in Fig. A.27. Furthermore, by optimizing the emitter currents and collector voltage, the MR of 2500 % is realized.

Here, bipolar transistors consist of two p-n junctions. First, MR of emitter-base junction is investigated, then MR of collector-base junction is also measured. As shown in Figs. A.32, A.33, A.34, and A.35, MR at 77 k in each junction is enhanced to 120 %, which is consistent with the MR of p-n Si diode measured in Section A.3.

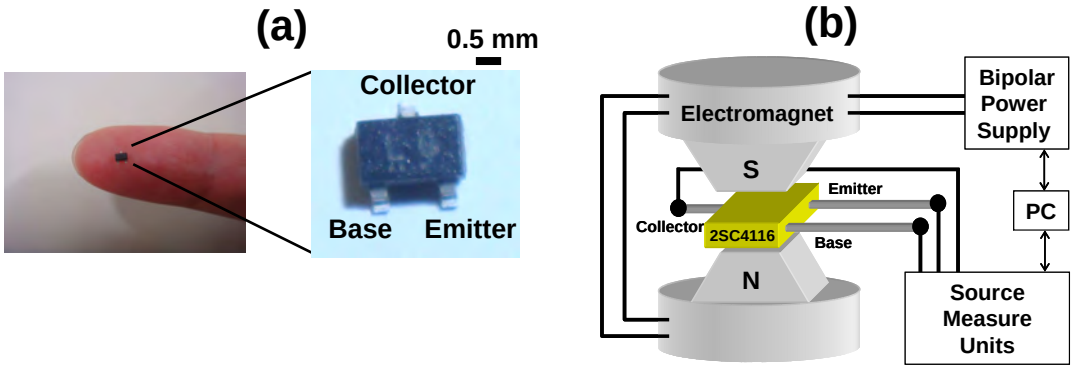


Fig. A.21. (a) Photograhph of NPN BT (2SC4116, TOSHIBA). (b) Schematic of NPN BT and direction of applied magnetic field *B*.

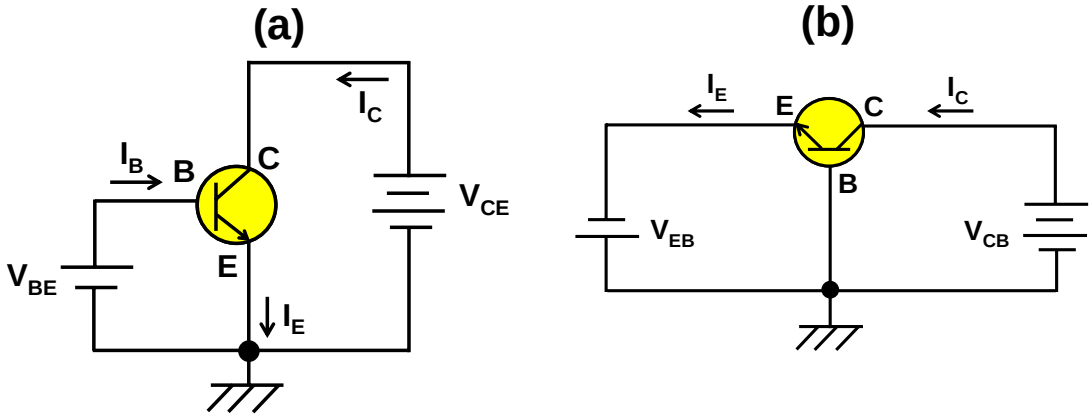


Fig. A.22. (a) Common-emitter configuration. (b) Common-base configuration.

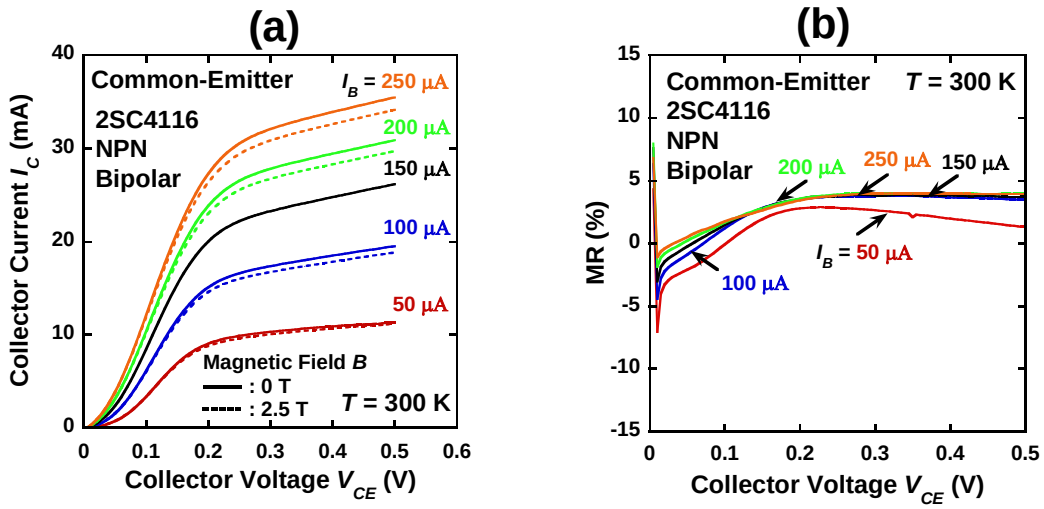


Fig. A.23. (a) Collector current I_C versus collector voltage V_{CE} characteristics of the bipolar transistor in the common-emitter with the applied magnetic field B of 0 and 2.5 T at 300 K. (b) MR dependence of bipolar transistor on collector voltage.

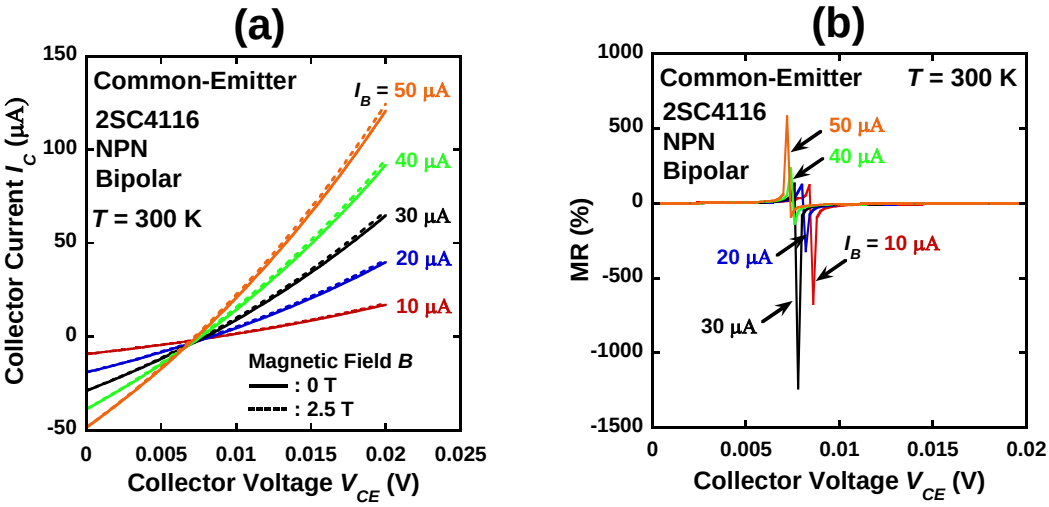


Fig. A.24. (a) At low collector voltage, Collector current I_C versus collector voltage V_{CE} characteristics of the bipolar transistor in the common-emitter with the applied magnetic field B of 0 and 2.5 T at 300 K. (b) MR dependence of bipolar transistor on collector voltage.

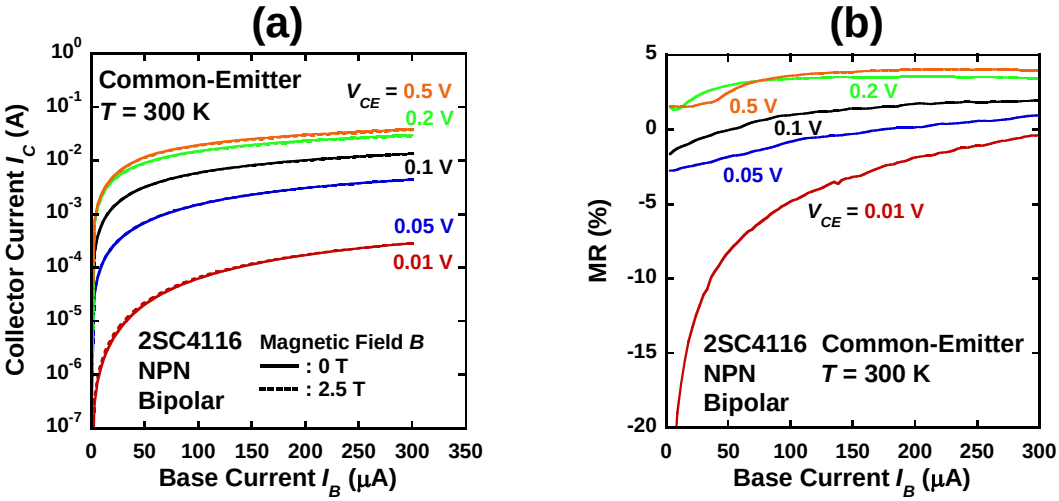


Fig. A.25. (a) Collector current versus base current transfer characteristics of the bipolar transistor for various collector voltages at 300 K. (b) MR of bipolar transistor in common-emitter as a function of base current.

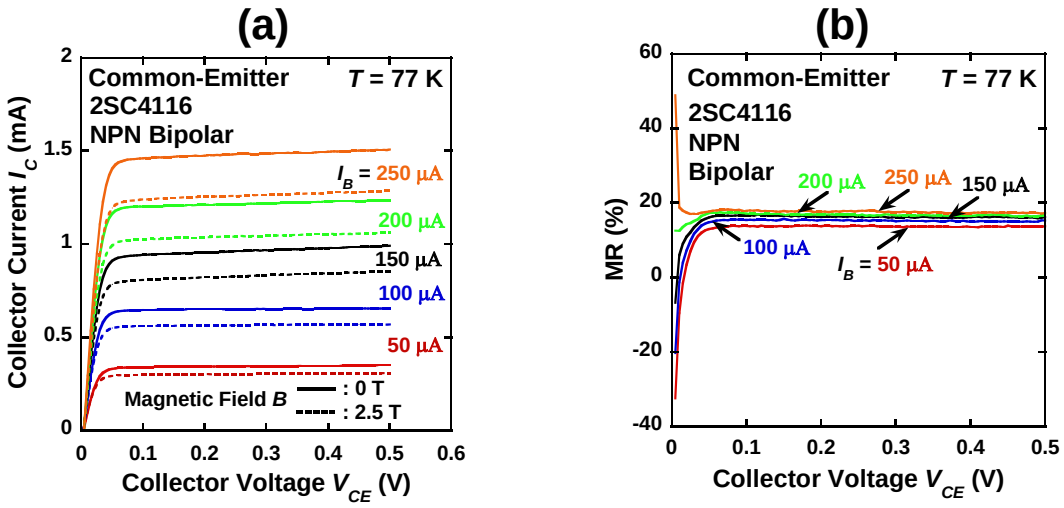


Fig. A.26. (a) (a) Collector current I_C versus collector voltage V_{CE} characteristics of the bipolar transistor in the common-emitter with the applied magnetic field B of 0 and 2.5 T at 77 K. (b) MR dependence of bipolar transistor on collector voltage.

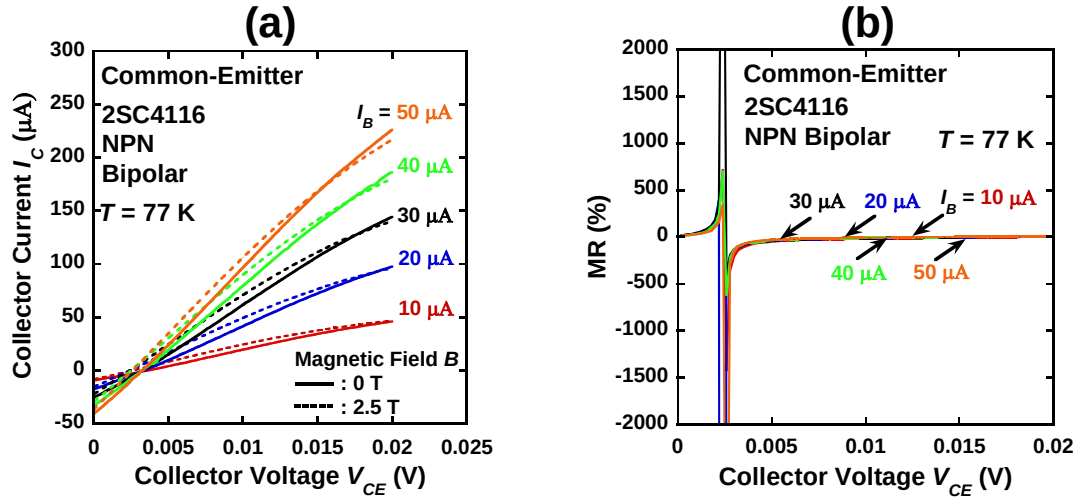


Fig. A.27. (a) At low collector voltage, Collector current I_C versus collector voltage V_{CE} characteristics of the bipolar transistor in the common-emitter with the applied magnetic field B of 0 and 2.5 T at 77 K. (b) MR dependence of bipolar transistor on collector voltage.

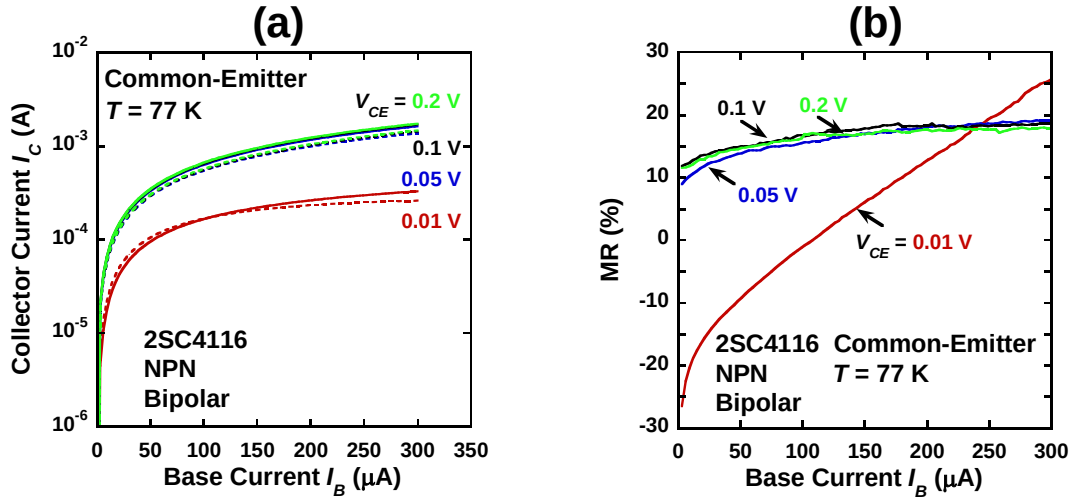


Fig. A.28. (a) (a) Collector current versus base current transfer characteristics of the bipolar transistor for various collector voltages at 77 K. (b) MR of bipolar transistor in common-emitter as a function of base current.

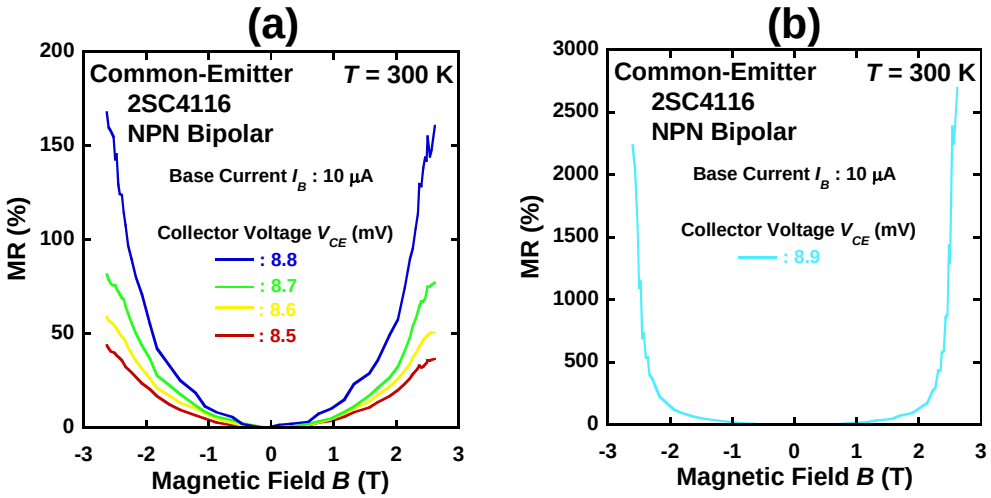


Fig. A.29. (a) MR of bipolar transistor as a function of magnetic field at 300 K. (b) MR of bipolar transistor at I_B = 10 μ A and V_{CE} = 8.9 mV as a function of magnetic field at 300 K.

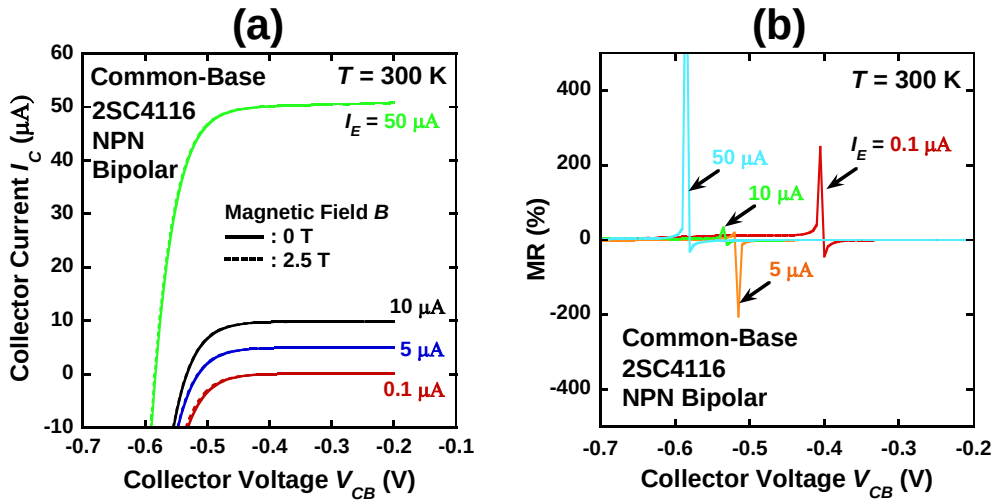


Fig. A.30. (a) Collector current I_C versus collector voltage V_{CE} characteristics of the bipolar transistor in the common-base with the applied magnetic field B of 0 and 2.5 T at 300 K. (b) MR dependence of bipolar transistor on collector voltage.

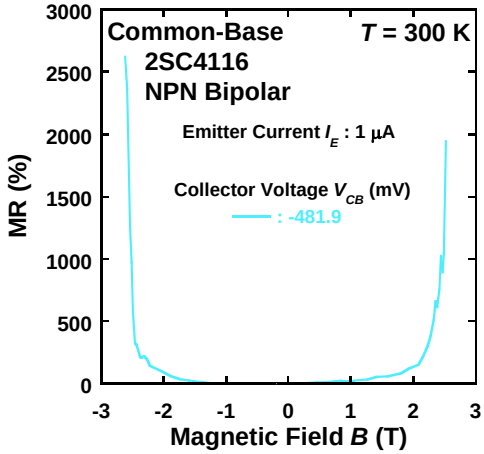


Fig. A.31. (a) MR of bipolar transistor at I_B = 1μA and V_{CE} = -481.9 mV as a function of magnetic field at 300 K.

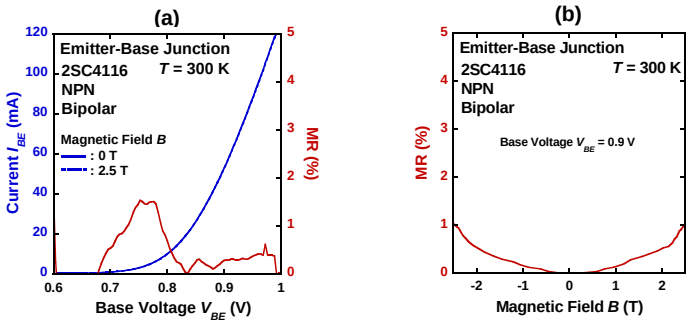


Fig. A.32. (a) Current and MR versus voltage characteristics of the emitter-base junction with the applied magnetic field *B* of 0 and 2.5 T at 300 K. (b) MR dependences of the emitter-base junction on the magnetic field with the voltage of 0.9 V.

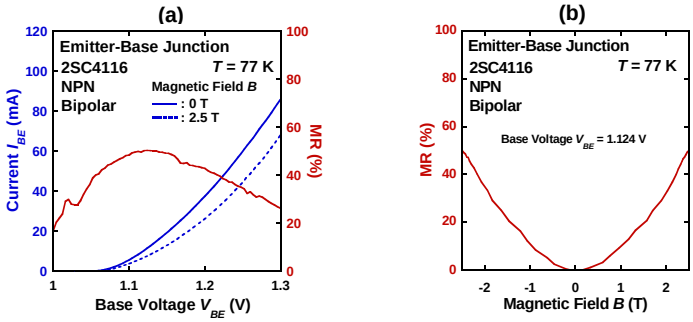


Fig. A.33. (a) Current and MR versus voltage characteristics of the emitter-base junction with the applied magnetic field *B* of 0 and 2.5 T at 77 K. (b) MR dependences of the emitter-base junction on the magnetic field with the voltage of 1.124 V.

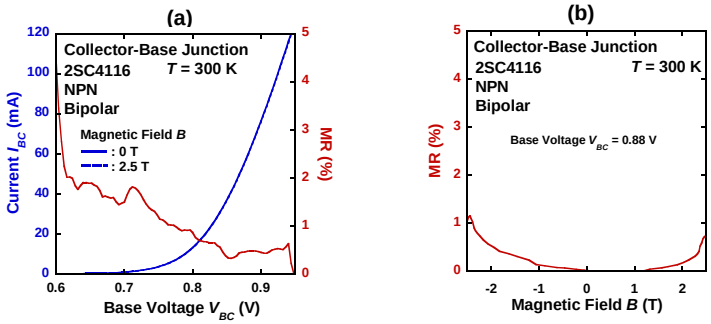


Fig. A.34. (a) Current and MR versus voltage characteristics of the collector-base junction with the applied magnetic field *B* of 0 and 2.5 T at 300 K. (b) MR dependences of the collector-base junction on the magnetic field with the voltage of 0.88 V.

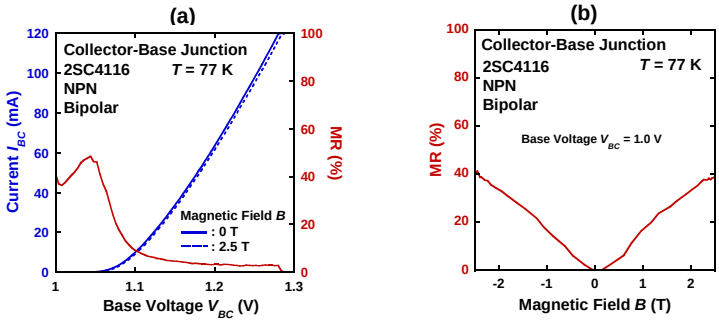


Fig. A.35. (a) Current and MR versus voltage characteristics of the collector-base junction with the applied magnetic field *B* of 0 and 2.5 T at 77 K. (b) MR dependences of the collector-base junction on the magnetic field with the voltage of 1.0 V.

A.5 Summary

MR effect of discrete Si transistors is investigated at 300 and 77 K. At the magnetic field of 2.2 T, the MOSFET and JFET show positive MR of 8 and 15 % at 300 K, respectively. In addition, MR of the MOSFET and JFET is enhanced to be 60 and 252 % at 77 K, respectively. The MR induced by a geometrical effect is expressed as $MR_{geo} = \mu^2 B^2$ x 100 %, and this fitting model provides a good fit to the experimental data with the electron mobilities of 1500 $cm^2V^{-1}s^{-1}$ for the MOSFET and 1800 $cm^2V^{-1}s^{-1}$ for the JFET at 300 K. Since the electron mobilities of discrete Si transistors are usually considered to be smaller than 1500-1800 $cm^2V^{-1}s^{-1}$ at 300 K, the enhancement ratio becomes almost same between the MOSFET and JFET at the value of 2.4 ~ 2.5. In addition, enhancement ratio of the MOSFET and JFET at 77 K is estimated to be almost same as those at 300 K. Therefore, the MR obtained in the transistors may be enhanced by physical MR effects such as impact ionization and space charge effect.

Furthermore, at room temperature, Si diode (1S2473, ROHM) and NPN BT (2SC4116, TOSHIBA) exhibit positive MR of 2, 3 % and MR at 77 K are enhanced to be 120, 15 %, respectively. Moreover, MR of BT at 300 K is reached 2500 % by optimizing the base current and applied bias voltage between collector and emitter.

Finally, Fig. A.36 shows the comparison of MR effects in semiconductor and ferromagnetic materials. From the figure, large MR effects are clearly observed in Si substrate and transistors. Hence, these results indicate that discrete Si transistors may be applicable for novel magnetoresistive functional devices.

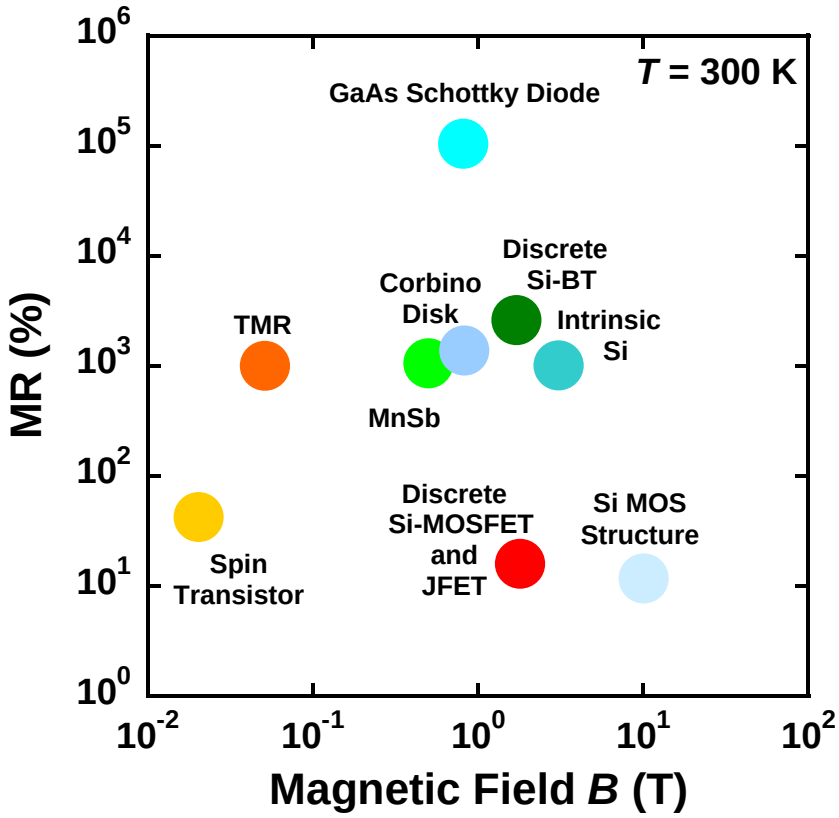


Fig. A.36. Comparison of MR effects in semiconductor and ferromagnetic materials.

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東京農工大学・電気通信大学 第 5 回合同シンポジウム「ナノ未来材料とコヒーレント光科学」、P40、2008 年 12 月 13 日、電気通信大学

11) 友田悠介、西村信也、白樫淳一、越田信義

“半導体・強磁性体へのナノスケール加工とデバイス応用”

科学研究費補助金特定領域研究

「シリコンナノエレクトロニクスの新展開　―ポストスケーリングテクノロジー―」第三回成果報告会、P107、2009 年 1 月 28 日-29 日、東京

12) 西村信也、白樫淳一

“10-nm スケール SPM リソグラフィー技術”

文部科学省大学院教育改革支援プログラム「科学立国人材育成プログラム」合宿コロキューム（研修会）、2009 年 3 月 7 日-8 日、ホテル エバーグリーン富士

13) 西村信也、古澤亜美、白樫淳一

“Research Activities on Nanoelectronics, Nanofabrication and Nanolithography”

女性未来育成機構「女子中高生のためのサマースクール 2009　農と工を一日でダブル体験 in 農工大」白樫研究室ポスター紹介 2009 年 8 月 1 日、東京農工大学

14) 西村信也、友田悠介、白樫淳一、越田信義

“半導体・強磁性体へのナノスケール加工とデバイス応用”

科学研究費補助金特定領域研究

「シリコンナノエレクトロニクスの新展開 ―ポストスケーリングテクノロジー―」第六回全体会議、P106、2009 年 8 月 6 日-7 日、名古屋

15) S. Nishimura, Y. Eto, T. Toyofuku, Y. Kuwabara and J. Shirakashi

“Control of Tunnel Resistance of Si Nanogaps Using Field-Emission-Induced Electromigration”

東京農工大学・電気通信大学 第 6 回合同シンポジウム「ナノ未来材料とコヒーレント光科学」、T78、2009 年 12 月 5 日、東京農工大学

16) 太田敢行、Bernard GELLOZ、友田悠介、西村信也、白樫淳一、越田信義
“シリコンナノ構造の電子機能”
科学研究費補助金特定領域研究
「シリコンナノエレクトロニクスの新展開　―ポストスケーリングテクノロジー―」第四回成果報告会、P106、2010 年 1 月 19 日-20 日、東京

17) S. Nishimura, R. Zaharuddin, Y. Kuwabara and J. Shirakashi
“Magnetoresistance Effects in Discrete Si Transistors”
東京農工大学・電気通信大学 第 7 回合同シンポジウム「ナノ未来材料とコヒーレント光科学」、T-43、2010 年 12 月 11 日、電気通信大学（発表予定）

18) 西村信也
平成 19 年度東京農工大学奨励奨学金奨学生
平成 19 年 3 月 26 日　授与

19) 西村信也
財団法人東電記念科学技術研究所 平成 19 年度学生研究奨励奨学生
平成 19 年 4 月 17 日　授与

20) 西村信也
東京農工大学研究奨励金制度「JIRITSU（自立）」
平成 20 年度リサーチフェロー
平成 20 年 4 月 4 日　授与

21) 西村信也
文部科学省 大学院教育改革支援プログラム
「科学立国人材育成プログラム」
平成 19～21 年度リサーチアシスタント
平成 19 年 11 月 1 日 ～ 平成 20 年 3 月 31 日
平成 20 年 4 月 1 日 ～ 平成 21 年 3 月 31 日
平成 21 年 4 月 8 日 ～ 平成 22 年 3 月 31 日

22) 西村信也

独立行政法人日本学術振興会　特別研究員

平成 21 年度採用（DC2）

平成 21 年 4 月 1 日 ~ 平成 23 年 3 月 31 日

< Awards >

1) T. Toyofuku, S. Nishimura, K. Miyashita and J. Shirakashi

(Selected for the Poster Award of TBN2008)

"10 Micrometer-Scale SPM Local Oxidation Lithography"

The 1st International Workshop on Tip-Based Nanofabrication (TBN2008), October 19-21, 2008, Taipei, Taiwan.